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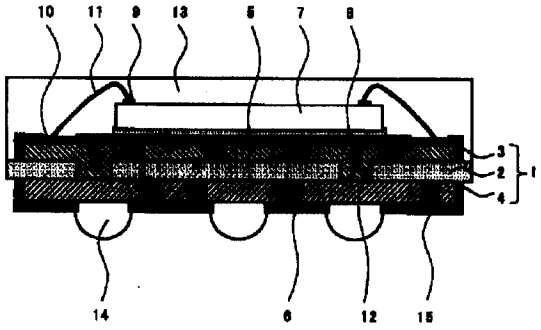
(54)【発明の名称】　回路装置およびその製造方法

(57)【要約】
【課題】　従来、導電パターンを持ったフレキシブルシートを支持基板として採用し、この上に半導体素子を実装し、全体をモールドした半導体装置が開発されている。この場合多層配線構造が形成できない問題や製造工程での絶縁樹脂シートの反りが顕著である問題を発生させる。
【解決手段】　第１の導電膜３と第２の導電膜４を絶縁樹脂２で貼り合わせた絶縁樹脂シートを用い、第１の導電膜３で第１の導電配線層５形成し、第２の導電膜４で第２の導電配線層６を形成し、両者を多層接続手段１２で接続する。半導体素子７は第１の導電配線層５を覆うオーバーコート樹脂８上に固着することで、第１の導電配線層５と第２の導電配線層６とで多層配線構造を実現する。また、厚く形成された第２の導電膜４があるため、熱膨張係数の違いにより発生する反りを防止することができる。



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【特許請求の範囲】

【請求項１】　第１の導電膜と、
第２の導電膜と、
前記第１の導電膜と前記第２の導電膜とをシート状に接着する絶縁樹脂と、
前記第１の導電膜をエッチングして形成された第１の導電配線層と、
前記第２の導電膜をエッチングして形成された第２の導電配線層と、
前記第１の導電配線層上に電気的に絶縁されて固着される半導体素子と、
前記第１の導電配線層と前記第２の導電配線層とを所望の個所で前記絶縁樹脂を貫通して接続する多層接続手段と、
前記第１の導電配線層および前記半導体素子を被覆する封止樹脂層と、
前記第２の導電配線層の所望個所に設けた外部電極とを具備することを特徴とした回路装置。

【請求項２】　前記第２の導電膜は第１の導電膜より厚く形成し支持強度を持たせることを特徴とする請求項１記載の回路装置。

【請求項３】　前記絶縁樹脂はポリイミド樹脂またはエポキシ樹脂を主成分とすることを特徴とする請求項１記載の回路装置。

【請求項４】　前記絶縁樹脂は前記第２の導電膜よりも薄いことを特徴とする請求項１記載の回路装置。

【請求項５】　前記半導体素子は前記第１の導電配線層上を被覆するオーバーコート樹脂上に固着されることを特徴とする請求項１記載の回路装置。

【請求項６】　前記多層接続手段は導電金属のメッキ膜であることを特徴とする請求項１記載の回路装置。

【請求項７】　前記第２の導電配線層のほとんどをオーバーコート樹脂で被覆し、該オーバーコート樹脂から露出された所望個所に半田より成る外部電極を設けたことを特徴とする請求項１記載の回路装置。

【請求項８】　第１の導電膜と第２の導電膜を絶縁樹脂で接着した絶縁樹脂シートを準備する工程と、
前記絶縁樹脂シートの所望個所に前記第１の導電膜および前記絶縁樹脂に貫通孔を形成し、前記第２の導電膜の裏面を選択的に露出する工程と、
前記貫通孔に多層接続手段を形成し、前記第１の導電膜と前記第２の導電膜を電気的に接続する工程と、
前記第１の導電膜を所望のパターンにエッチングして第１の導電配線層を形成する工程と、
前記第１の導電配線層上に電気的に絶縁して半導体素子を固着する工程と、
前記第１の導電配線層および前記半導体素子を封止樹脂層で被覆する工程と、
前記第２の導電膜を所望のパターンにエッチングして第２の導電配線層を形成する工程と、

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前記第２の導電配線層の所望個所に外部電極を形成する工程とを具備することを特徴とする回路装置の製造方法。

【請求項９】　前記第１の導電膜および前記第２の導電膜は銅箔で形成されることを特徴とする請求項８記載の回路装置の製造方法。

【請求項１０】　前記第１の導電膜は前記第２の導電膜より薄く形成され、前記第１の導電配線層を微細パターン化することを特徴とする請求項８記載の回路装置の製造方法。

【請求項１１】　前記第２の導電膜は前記第１の導電膜より厚く形成され、前記封止樹脂層で被覆する工程まで前記第２の導電膜で機械的に支持することを特徴とする請求項８記載の回路装置の製造方法。

【請求項１２】　前記封止樹脂層で被覆する工程後では前記封止樹脂層で機械的に支持することを特徴とする請求項８記載の回路装置の製造方法。

【請求項１３】　前記貫通孔は前記第１の導電膜をエッチングした後に、前記第１の導電膜をマスクとして前記絶縁樹脂をレーザーエッチングすることを特徴とする請求項８記載の回路装置の製造方法。

【請求項１４】　前記レーザーエッチングは炭酸ガスレーザーを用いることを特徴とする請求項１３記載の回路装置の製造方法。

【請求項１５】　前記多層接続手段は導電金属の無電界メッキおよび電界メッキで前記貫通孔および前記第１の導電膜の表面に形成されることを特徴とする請求項８記載の回路装置の製造方法。

【請求項１６】　前記第１の導電配線層を形成後、所望の個所を残してオーバーコート樹脂で被覆することを特徴とする請求項８記載の回路装置の製造方法。

【請求項１７】　前記第１の導電配線層の所望の個所に金あるいは銀のメッキ層を形成することを特徴とする請求項１６記載の回路装置の製造方法。

【請求項１８】　前記オーバーコート樹脂上に前記半導体素子を固着することを特徴とする請求項１６記載の回路装置の製造方法。

【請求項１９】　前記半導体素子の電極と前記金あるいは銀のメッキ層とをボンディングワイヤで接続することを特徴とする請求項１７記載の回路装置の製造方法。

【請求項２０】　前記封止樹脂層はトランスファーモールドで形成されることを特徴とする請求項８記載の回路装置の製造方法。

【請求項２１】　前記第２の導電配線層のほとんどをオーバーコート樹脂で被覆することを特徴とする請求項８記載の回路装置の製造方法。

【請求項２２】　前記外部電極は半田のスクリーン印刷で半田を付着し、加熱溶融して形成されることを特徴とする請求項８記載の回路装置の製造方法。

【請求項２３】　前記外部電極は半田のリフローで形成

されることを特徴とする請求項８記載の回路装置の製造方法。

【請求項２４】　前記外部電極は前記第２の導電膜を所望のパターンにエッチングしその表面を金あるいはパラジウムメッキされて形成されることを特徴とする請求項８記載の回路装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、回路装置およびその製造方法に関し、特に２枚の導電膜を用いた薄型で多層配線も実現できる回路装置およびその製造方法に関するものである。

【０００２】

【従来の技術】近年、ＩＣパッケージは携帯機器や小型・高密度実装機器への採用が進み、従来のＩＣパッケージとその実装概念が大きく変わろうとしている。例えば特開２０００－１３３６７８号公報に述べられている。これは、絶縁樹脂シートの一例としてフレキシブルシートであるポリイミド樹脂シートを採用した半導体装置に関する技術である。

【０００３】図１２～図１４は、フレキシブルシート５０をインターポーザー基板として採用するものである。尚、各図の上に示す図面は、平面図、下に示す図面は、Ａ－Ａ線の断面図である。

【０００４】まず図１２に示すフレキシブルシート５０の上には、接着剤を介して銅箔パターン５１が貼り合わされて用意されている。この銅箔パターン５１は、実装される半導体素子がトランジスタ、ＩＣにより、そのパターンが異なるが、一般には、ボンディングパッド５１Ａ、アイランド５１Ｂが形成されている。また符号５２は、フレキシブルシート５０の裏面から電極を取り出すための開口部であり、前記銅箔パターン５１が露出している。

【０００５】続いて、このフレキシブルシート５０は、ダイボンダーに搬送され、図１３の如く、半導体素子５３が実装される。その後、このフレキシブルシート５０は、ワイヤーボンダーに搬送され、ボンディングパッド５１Ａと半導体素子５３のパッドが金属細線５４で電気的に接続されている。

【０００６】最後に、図１４（Ａ）の如く、フレキシブルシート５０の表面に封止樹脂５５が設けられて封止される。ここでは、ボンディングパッド５１Ａ、アイランド５１Ｂ、半導体素子５３および金属細線５４を被覆するようにトランスファーモールドされる。

【０００７】その後、図１４（Ｂ）に示すように、半田や半田ボール等の接続手段５６が設けられ、半田リフロー炉を通過することで開口部５２を介してボンディングパッド５１Ａと融着した球状の半田５６が形成される。しかもフレキシブルシート５０には、半導体素子５３がマトリックス状に形成されるため、図１４の様にダイシングされ、個々に分離される。

【０００８】また図１４（Ｃ）に示す断面図は、フレキシブルシート５０の両面に電極として５１Ａと５１Ｄが形成されているものである。このフレキシブルシート５０は、一般に、両面がパターニングされてメーカーから供給されている。

【０００９】

【発明が解決しようとする課題】上述したフレキシブルシート５０を用いた半導体装置は周知の金属フレームを用いないので、極めて小型で薄型のパッケージ構造を実現できる利点を有するが、実質的にフレキシブルシート５０の表面に設けた１層の銅箔パターン５１のみで配線を行うので多層配線構造を実現できない問題点があった。

【００１０】また多層配線構造を実現するには支持強度を保つために、フレキシブルシート５０を約２００μｍと十分に厚くする必要があり、薄型化に逆行する問題点も有していた。

【００１１】更に製造方法においては、前述した製造装置、例えばダイボンター、ワイヤーボンダー、トランスファーモールド装置、リフロー炉等に於いて、フレキシブルシート５０が搬送されて、ステージまたはテーブルと言われる部分に装着される。

【００１２】しかしフレキシブルシート５０のベースとなる絶縁樹脂の厚みは５０μｍ程度と薄くすると、表面に形成される銅箔パターン５１の厚みも９～３５μｍと薄い場合、図１５に示すように反ったりして搬送性が非常に悪く、また前述したステージやテーブルへの装着性が悪い欠点があった。これは、絶縁樹脂自身が非常に薄いために依る反り、銅箔パターン５１と絶縁樹脂との熱膨張係数との差による反りが考えられる。特にガラスクロス繊維の芯材のない堅い絶縁材料が、図１５に示すように反っていると、上からの加圧で簡単に割れてしまう問題点があった。

【００１３】また開口部５２の部分は、モールドの際に上から加圧されるため、ボンディングパッド５１Ａの周辺を上に反らせる力が働き、ボンディングパッド５１Ａの接着性を悪化させることもあった。

【００１４】またフレキシブルシート５０を構成する樹脂材料自身にフレキシブル性が無かったり、熱伝導性を高めるためにフィラーを混入すると、堅くなる。この状態でワイヤーボンダーでボンディングするとボンディング部分にクラックが入る場合がある。またトランスファーモールドの際も、金型が当接する部分でクラックが入る場合がある。これは図１５に示すように反りがあるとより顕著に現れる。

【００１５】今まで説明したフレキシブルシート５０は、裏面に電極が形成されないものであったが、図１４（Ｃ）に示すように、フレキシブルシート５０の裏面にも電極５１Ｄが形成される場合もある。この時、電極５

１Ｄが前記製造装置と当接したり、この製造装置間の搬送手段の搬送面と当接するため、電極５１Ｄの裏面に損傷が発生する問題があった。この損傷が入ったままで電極として成るため、後に熱が加わったりすることにより電極５１Ｄ自身にクラックが入る問題点もあった。

【００１６】またフレキシブルシート５０の裏面に電極５１Ｄが設けられると、トランスファーモールドの際、ステージに面接触できない問題点が発生する。この場合、前述したようにフレキシブルシート５０が堅い材料で成ると、電極５１Ｄが支点となり、電極５１Ｄの周囲が下方に加圧されるため、フレキシブルシート５０にクラックを発生させる問題点があった。

【００１７】

【課題を解決するための手段】本発明は上記の課題に鑑みてなされ、第１に構造上では、第１の導電膜と、第２の導電膜と、前記第１の導電膜と前記第２の導電膜とをシート状に接着する絶縁樹脂と、前記第１の導電膜をエッチングして形成された第１の導電配線層と、前記第２の導電膜をエッチングして形成された第２の導電配線層と、前記第１の導電配線層上に電気的に絶縁されて固着される半導体素子と、前記第１の導電配線層と前記第２の導電配線層とを所望の個所で前記絶縁樹脂を貫通して接続する多層接続手段と、前記第１の導電配線層および前記半導体素子を被覆する封止樹脂層と、前記第２の導電配線層の所望個所に設けた外部電極とを具備する回路装置により解決するものである。

【００１８】第１の導電膜と第２の導電膜を極めて薄い絶縁樹脂で電気的に絶縁するとともに物理的には一体化したシートを実現し、第１の導電膜で第１の導電配線層を形成し、第２の導電膜で第２の導電配線層を形成し、多層接続手段で第１の導電配線層と第２の導電配線層を接続して多層配線構造を実現している。

【００１９】また半導体素子はオーバーコート樹脂で第１の導電配線層と電気的に絶縁して固着されるので、半導体素子下部に第１の導電配線層を自由に引き回しできる。

【００２０】第２に製造方法上では、第１の導電膜と第２の導電膜を絶縁樹脂で接着した回路基板を準備する工程と、前記回路基板の所望個所に前記第１の導電膜および前記絶縁樹脂に貫通孔を形成し、前記第２の導電膜を選択的に露出する工程と、前記貫通孔に多層接続手段を形成し、前記第１の導電膜と前記第２の導電膜を電気的に接続する工程と、前記第１の導電膜を所望のパターンにエッチングして第１の導電配線層を形成する工程と、前記第１の導電配線層上に電気的に絶縁して半導体素子を固着する工程と、前記第１の導電配線層および前記半導体素子を封止樹脂層で被覆する工程と、前記第２の導電膜を所望のパターンにエッチングして第２の導電配線層を形成する工程と、前記第２の導電配線層の所望個所に外部電極を形成する工程とを具備することにより上記の課題を解決する。

【００２１】第１の導電膜および第２の導電膜で厚く形成されるため、絶縁樹脂が薄くてもシート状の回路基板のフラット性が維持できる。

【００２２】また、第１の導電配線層および半導体素子を封止樹脂層で被覆する工程までは、第２の導電膜で機械的強度を持たせ、その後は封止樹脂層で機械的強度を持たせるので第２の導電膜で第２の導電配線層を容易に形成できる。この結果絶縁樹脂は機械的強度は必要なく、電気的絶縁を保持できる厚みまで薄くすることができる。

【００２３】更に、トランスファーモールド装置の下金型と面で第２の導電膜全体と接触できるため、局部的な加圧が無くなり絶縁樹脂のクラック発生を抑止することができる。

【００２４】更にまた、第１の導電膜は貫通孔に多層接続手段を形成した後に、第１の導電配線層を形成するので、マスクなしで多層接続手段を形成できる。

【００２５】

【発明の実施の形態】回路装置を説明する第１の実施の形態本発明に依る回路装置は、図１に示す如く、第１の導電膜３と、第２の導電膜４と、前記第１の導電膜３と前記第２の導電膜４とをシート状に接着する絶縁樹脂２と、前記第１の導電膜３をエッチングして形成された第１の導電配線層５と、前記第２の導電膜４をエッチングして形成された第２の導電配線層６と、前記第１の導電配線層５上に電気的に絶縁されて固着される半導体素子７と、前記第１の導電配線層５と前記第２の導電配線層６とを所望の個所で前記絶縁樹脂２を貫通して接続する多層接続手段１２と、前記第１の導電配線層５および前記半導体素子７を被覆する封止樹脂層１３と、前記第２の導電配線層６の所望個所に設けた外部電極１４とから構成されている。

【００２６】まず絶縁樹脂シートについて説明する。図３は、全体が絶縁樹脂シート１であり、中間には絶縁樹脂２が設けられている。この絶縁樹脂２の表面には第１の導電膜３が形成され、裏面には第２の導電膜４が形成される。

【００２７】つまり絶縁樹脂シート１の表面には実質全域に第１の導電膜３が形成され、裏面にも実質全域に第２の導電膜４が形成されるものである。また絶縁樹脂２の材料は、ポリイミド樹脂またはエポキシ樹脂等の高分子から成る絶縁材料で成る。また、第１の導電膜３および第２の導電膜４は、好ましくは、Ｃｕを主材料とするもの、または公知のリードフレームの材料であり、メッキ法、蒸着法またはスパッタ法で絶縁樹脂２に被覆されたり、圧延法やメッキ法により形成された金属箔が貼着されても良い。

【００２８】また絶縁樹脂シート１は、キャスティング法で形成されても良い。以下に簡単にその製造方法を述

べる。まず平膜状の第１の導電膜の上に糊状のポリイミド樹脂を塗布し、また平膜状の第２の導電膜の上にも糊状のポリイミド樹脂を塗布する。そして両者のポリイミドを半硬化させた後に貼り合わせると絶縁樹脂シート１ができあがる。従って、絶縁樹脂シート１には補強用のガラスクロス繊維を不要としている。

【００２９】本発明の特徴とする点は、第２の導電膜４を第１の導電膜３よりも厚く形成するところにある。

【００３０】第１の導電膜３は厚さが５～３５μｍ程度に形成され、できるだけ薄くしてファインパターンが形成できるように配慮される。第２の導電膜４は厚さが７０～２００μｍ程度で良く、支持強度を持たせる点が重視される。

【００３１】従って、第２の導電膜４を厚く形成することにより、絶縁樹脂シート１の平坦性を維持でき、後の工程の作業性を向上させ、絶縁樹脂２への欠陥、クラック等の誘発を防止することができる。

【００３２】また平坦性を維持しながら封止樹脂を硬化できるので、パケッジの裏面も平坦にでき、絶縁樹脂シート１の裏面に形成される電極もフラットに配置できる。よって、実装基板上の電極と絶縁樹脂シート１裏面の電極とを当接でき、半田不良を防止することができる。

【００３３】絶縁樹脂２は、ポリイミド樹脂、エポキシ樹脂等が好ましい。ペースト状のものを塗ってシートとするキャスティング法の場合、その膜厚は、１０μｍ～１００μｍ程度である。またシートとして形成する場合、市販のものは２５μｍが最小の膜厚である。また熱伝導性が考慮され、中にフィラーが混入されても良い。材料としては、ガラス、酸化Ｓｉ、酸化アルミニウム、窒化Ａｌ、Ｓｉカーバイド、窒化ボロン等が考えられる。

【００３４】このように絶縁樹脂２は上述したフィラーを混入した低熱抵抗樹脂、超低熱抵抗樹脂あるいはポリイミド樹脂と選択でき、形成する回路装置の性質により使い分けることができる。

【００３５】第１の導電配線層５は第１の導電膜３をエッチングして形成される。第１の導電膜３は厚さが５～３５μｍ程度に形成され、エッチングにより周辺にボンデイングパッド１０とこのボンデイングパッド１０から中央に延在される第１の導電配線層５とが形成される。搭載される半導体素子のパッド数が多くなればなるほどファインパターン化が要求される。

【００３６】第２の導電配線層６は第２の導電膜をエッチングして形成される。第２の導電膜４の膜厚は、７０μｍ～２００μｍ程度であり、ファインパターンには適さないが、外部電極１４の形成が主であり、必要に応じて多層配線を形成できる。

【００３７】半導体素子７は第１の導電配線層５上を被覆するオーバーコート樹脂８上に接着剤で固着され、半導体素子７と第１の導電配線層５とは電気的に絶縁されている。この結果、半導体素子７の下にはファインパターンの第１の導電配線層５が自由に配線でき、配線の自由度が大幅に増大する。半導体素子７の各電極パッド９は周辺に設けた第１の導電配線層５の一部であるボンデイングパッド１０にボンディングワイヤー１１で接続されている。なお、ボンデイングパッド１０はボンディングが行えるように金あるいは銀メッキが表面に施されている。

【００３８】多層接続手段１２は第１の導電配線層５と第２の導電配線層６とを所望の個所で絶縁樹脂２を貫通して接続している。多層配線手段１２としては具体的には銅のメッキ膜が適している。また金、銀、パラジュウム等のメッキ膜でも良い。

【００３９】封止樹脂層１３は第１の導電配線層５および半導体素子７を被覆している。この封止樹脂層１３は完成した回路装置の機械的支持の働きも兼用している。

【００４０】外部電極１４は第２の導電配線層６の所望個所に設けられる。すなわち、第２の導電配線層６の大部分はオーバーコート樹脂１５で被覆され、露出した第２の導電配線層６上に半田で形成された外部電極１４を設ける。

【００４１】図２を参照して、具体化された本発明の回路装置を説明する。まず、実線で示すパターンは第１の導電配線層５であり、点線で示すパターンは第２の導電配線層６である。第１の導電配線層５は半導体素子７を取り巻くようにボンディングパッド１０が周辺に設けられ、一部では２段に配置されて多パッドを有する半導体素子７に対応している。ボンディングパッド１０は半導体素子７の対応する電極パッド９とボンディングワイヤー１１で接続され、ボンディングパッド１０からファインパターンの第１の導電配線層５が半導体素子７の下に多数延在されて、黒丸で示す多層接続手段１２で第２の導電配線層６と接続されている。

【００４２】斯かる構造であれば、２００以上パッドを有する半導体素子でも、第１の導電配線層５のファインパターンを利用して所望の第２の導電配線層６まで多層配線構造で延在でき、第２の導電配線層６に設けられた外部電極１４から外部回路への接続が行える。回路装置の製造方法を説明する第２の実施の形態本発明の回路装置の製造方法について、図１～図１０を参照して説明する。

【００４３】本発明の回路装置の製造方法は、第１の導電膜３と第２の導電膜４を絶縁樹脂２で接着した絶縁樹脂シート１を準備する工程と、前記絶縁樹脂シート１の所望個所に前記第１の導電膜３および前記絶縁樹脂２に貫通孔２１を形成し、前記第２の導電膜４の裏面を選択的に露出する工程と、前記貫通孔２１に多層接続手段１２を形成し、前記第１の導電膜３と前記第２の導電膜４を電気的に接続する工程と、前記第１の導電膜３を所望

のパターンにエッチングして第１の導電配線層５を形成する工程と、前記第１の導電配線層５上に電気的に絶縁して半導体素子７を固着する工程と、前記第１の導電配線層５および前記半導体素子７を封止樹脂層１３で被覆する工程と、前記第２の導電膜４を所望のパターンにエッチングして第２の導電配線層６を形成する工程と、前記第２の導電配線層６の所望個所に外部電極１４を形成する工程から構成されている。

【００４４】本発明の第１の工程は、図３に示すように、第１の導電膜３と第２の導電膜４を絶縁樹脂２で接着した絶縁樹脂シート１を準備することにある。

【００４５】絶縁樹脂シート１の表面は、実質全域に第１の導電膜３が形成され、裏面にも実質全域に第２の導電膜４が形成されるものである。また絶縁樹脂２の材料は、ポリイミド樹脂またはエポキシ樹脂等の高分子から成る絶縁材料で成る。また、第１の導電膜３および第２の導電膜４は、好ましくは、Ｃｕを主材料とするもの、または公知のリードフレームの材料であり、メッキ法、蒸着法またはスパッタ法で絶縁樹脂２に被覆されたり、圧延法やメッキ法により形成された金属箔が貼着されても良い。

【００４６】また絶縁樹脂シート１は、キャスティング法で形成されても良い。以下に簡単にその製造方法を述べる。まず平膜状の第１の導電膜３の上に糊状のポリイミド樹脂を塗布し、また平膜状の第２の導電膜４の上にも糊状のポリイミド樹脂を塗布する。そして両者のポリイミド樹脂を半硬化させた後に貼り合わせると絶縁樹脂シート１ができあがる。

【００４７】本発明の特徴とする点は、第２の導電膜４を第１の導電膜３よりも厚く形成するところにある。

【００４８】第１の導電膜３は厚さが５～３５μｍ程度に形成され、できるだけ薄くしてファインパターンが形成できるように配慮される。第２の導電膜４は厚さが７０～２００μｍ程度で良く、支持強度を持たせる点が重視される。

【００４９】絶縁樹脂２は、ポリイミド樹脂、エポキシ樹脂等が好ましい。ペースト状のものを塗ってシートとするキャスティング法の場合、その膜厚は、１０μｍ～１００μｍ程度である。またシートとして形成する場合、市販のものは２５μｍが最小の膜厚である。また熱伝導性が考慮され、中にフィラーが混入されても良い。材料としては、ガラス、酸化Ｓｉ、酸化アルミニウム、窒化Ａｌ、Ｓｉカーバイド、窒化ボロン等が考えられる。

【００５０】このように絶縁樹脂２は上述したフィラーを混入した低熱抵抗樹脂、超低熱抵抗樹脂あるいはポリイミド樹脂と選択でき、形成する回路装置の性質により使い分けることができる。

【００５１】本発明の第２の工程は、図４に示す如く、絶縁樹脂シート１の所望個所に第１の導電膜３および絶縁樹脂２に貫通孔２１を形成し、第２の導電膜４を選択的に露出することにある。

【００５２】第１の導電膜３の貫通孔２１を形成する部分だけを露出してホトレジストで全面を被覆する。そしてこのホトレジストを介して第１の導電膜３をエッチングする。第１の導電膜３はＣｕを主材料とするものであるので、エッチング液は、塩化第２鉄または塩化第２銅を用いてケミカルエッチングを行う。貫通孔２１の開口径は、ホトリソグラフィーの解像度により変化するが、ここでは５０～１００μｍ程度である。またこのエッチングの際に、第２の導電膜４は接着性のシート等でカバーしてエッチング液から保護する。しかし第２の導電膜４自体が十分に厚く、エッチング後にも平坦性が維持できる膜厚であれば、少々エッチングされても構わない。なお、第１の導電膜３としてはＡｌ、Ｆｅ、Ｆｅ－Ｎｉ、公知のリードフレーム材等でも良い。

【００５３】続いて、ホトレジストを取り除いた後、第１の導電膜３をマスクにして、レーザーにより貫通孔２１の真下の絶縁樹脂２を取り除き、貫通孔２１の底に第２の導電膜４の裏面を露出させる。レーザーとしては、炭酸ガスレーザーが好ましい。またレーザーで絶縁樹脂を蒸発させた後、開口部の底部に残査がある場合は、過マンガン酸ソーダまたは過硫酸アンモニウム等でウェットエッチングし、この残査を取り除く。

【００５４】なお、本工程では第１の導電膜３が１０μｍ程度と薄い場合、ホトレジストで貫通孔２１以外を被覆した後に炭酸ガスレーザーで第１の導電膜３および絶縁樹脂２を一括して貫通孔２１を形成できる。この場合には予め第１の導電膜３の表面を粗化する黒化処理工程が必要である。

【００５５】本発明の第３の工程は、図５に示す如く、貫通孔２１に多層接続手段１２を形成し、第１の導電膜３と第２の導電膜４を電気的に接続することにある。

【００５６】貫通孔２１を含む第１の導電膜３全面に第２の導電膜４と第１の導電膜３の電気的接続を行う多層接続手段１２であるメッキ膜を形成する。このメッキ膜は無電解メッキと電解メッキの両方で形成され、ここでは、無電解メッキにより約２μｍのＣｕを少なくとも貫通孔２１を含む第１の導電膜３全面に形成する。これにより第１の導電膜３と第２の導電膜４が電気的に導通するため、再度この第１および第２導電膜３，４を電極にして電解メッキを行い、約２０μｍのＣｕをメッキする。これにより貫通孔２１はＣｕで埋め込まれ、多層接続手段１２が形成される。なお、商品名でエバラユージライトというメッキ液を採用すると、貫通孔２１のみを選択的に埋め込むことも可能である。またメッキ膜は、ここではＣｕを採用したが、Ａｕ、Ａｇ、Ｐｄ等を採用しても良い。またマスクを使用して部分メッキをしても良い。

【００５７】本発明の第４の工程は、図６および図７に

示す如く、第１の導電膜３を所望のパターンにエッチングして第１の導電配線層５を形成することにある。

【００５８】第１の導電膜３上に所望のパターンのホトレジストで被覆し、ボンディングパッド１０およびボンディングパッド１０から中央に延在される第１の導電配線層５をケミカルエッチングにより形成する。第１の導電膜３はＣｕを主材料とするものであるので、エッチング液は、塩化第２鉄または塩化第２銅を用いれば良い。

【００５９】第１の導電膜３は厚さが５～３５μｍ程度に形成されているので、第１の導電配線層５は５０μｍ以下のファインパターンに形成できる。

【００６０】続いて、第１の導電配線層５のボンディングパッド１０を露出して他の部分をオーバーコート樹脂８で被覆する。オーバーコート樹脂８は溶剤で溶かしたエポキシ樹脂等をスクリーン印刷で付着し、熱硬化させる。

【００６１】また、図７に示す如く、ボンディングパッド１０上にはボンディング性を考慮して、Ａｕ、Ａｇ等のメッキ膜２２が形成される。このメッキ膜２２はオーバーコート樹脂８をマスクとしてボンディングパッド１０上に選択的に無電界メッキで付着されるか、また第２の導電膜４を電極として電界メッキで付着される。

【００６２】本発明の第５の工程は、図８に示す如く、第１の導電配線層５上に電気的に絶縁して半導体素子７を固着することにある。

【００６３】半導体素子７はベアチップのままオーバーコート樹脂８上に絶縁性接着樹脂２５でダイボンドされる。半導体素子７とその下の第１の導電配線層５とはオーバーコート樹脂８で電気的に絶縁されるので、第１の導電配線層５は半導体素子７の下でも自由に配線でき、多層配線構造を実現できる。

【００６４】また、半導体素子７の各電極パッド９は周辺に設けた第１の導電配線層５の一部であるボンディングパッド１０にボンディングワイヤー１１で接続されている。半導体素子７はフェイスダウンで実装されても良い。この場合、半導体素子７の各電極パッド９表面に半田ボールやバンプが設けられ、絶縁樹脂シート１の表面には半田ボールの位置に対応した部分にボンディングパッド１０と同様の電極が設けられる（図１１参照）。

【００６５】ワイヤーボンデインクの時の絶縁樹脂シート１を用いるメリットについて述べる。一般にＡｕ線のワイヤーボンディングの際は、２００℃～３００℃に加熱される。この時、第２の導電膜４が薄いと、絶縁樹脂シート１が反り、この状態でボンディングヘッドを介して絶縁樹脂シート１が加圧されると、絶縁樹脂シート１に亀裂の発生する可能性がある。これは絶縁樹脂２にフィラーが混入されると、材料自体が堅くなり柔軟性を失うため、より顕著に現れる。また樹脂は金属から比べると柔らかいので、ＡｕやＡｌのボンディングでは、加圧や超音波のエネルギーが発散してしまう。しかし、絶縁樹脂２を薄く且つ第２の導電膜４自体が厚く形成されることでこれらの問題を解決することができる。

【００６６】本発明の第６の工程は、図９に示す如く、第１の導電配線層５および半導体素子７を封止樹脂層１３で被覆することにある。

【００６７】絶縁樹脂シート１は、モールド装置にセットされて樹脂モールドを行う。モールド方法としては、トランスファーモールド、インジェクションモールド、塗布、ディピング等でも可能である。しかし、量産性を考慮すると、トランスファーモールド、インジェクションモールドが適している。

【００６８】本工程では、モールドキャビティーの下金型に絶縁樹脂シート１はフラットで当接される必要があるが、厚い第２の導電膜４がこの働きをする。しかもモールドキャビティーから取り出した後も、封止樹脂層１３の収縮が完全に完了するまで、第２の導電膜４によってパッケージの平坦性を維持している。

【００６９】すなわち、本工程までの絶縁樹脂シート１の機械的支持の役割は第２の導電膜４により担われている。

【００７０】本発明の第７の工程は、図１０に示す如く、第２の導電膜４を所望のパターンにエッチングして第２の導電配線層６を形成することにある。

【００７１】第２の導電膜４は、所望のパターンのホトレジストで被覆し、ケミカルエッチングで第２の導電配線層６を形成する。第２の導電膜４は厚いのでファインパターン化には適していないが、大部分が外部電極１４を形成する目的であり問題はない。第２の導電配線層６は図２に示すように一定の間隔で配列され、個々は第１の導電配線層５と多層接続手段１２を介して電気的に接続されて多層配線構造を実現している。なお必要であれば余白部分で第１の導電配線層５を交差させるための第２の導電配線層６を形成しても良い。

【００７２】本発明の第８の工程は、図１に示す如く、第２の導電配線層６の所望個所に外部電極１４を形成することにある。

【００７３】第２の導電配線層１５は外部電極１４を形成する部分を露出して溶剤で溶かしたエポキシ樹脂等をスクリーン印刷してオーバーコート樹脂１５で大部分を被覆する。次に半田のリフローによりこの露出部分に外部電極１４を同時に形成する。

【００７４】最後に、絶縁樹脂シート１には回路装置が多数マトリックス状に形成されているので、封止樹脂層１３および絶縁樹脂シート１をダイシングしてそれらを個々の回路装置に分離する。

【００７５】図１１に半導体素子７はフェイスダウンで実装された構造を示す。図１と共通する構成要素は同一符号を付している。半導体素子７にはバンプ電極３１が設けられ、このバンプ電極３１とパッド電極１０とが接続される。オーバーコート樹脂８と半導体素子７の隙間

はアンダーフィル樹脂３２で充填される。この構造ではボンディングワイヤーを無くすることができ、封止樹脂層１３の厚みを更に薄くできる。また外部電極１４は第２の導電膜４をエッチングしてその表面を金あるいはパラジウムメッキ膜３３で被覆したバンプ電極でも達成できる。

【００７６】

【発明の効果】本発明に依れば、構造上では以下の利点を有する。

【００７７】第１に、第１の導電膜を薄く形成されているため、第１の導電配線層がファインパターン化でき、電極パッド数が１００以上の半導体素子の組み込みが可能となる。

【００７８】第２に、オーバーコート樹脂で半導体素子と第１の導電配線層とを電気的に絶縁できるので、半導体素子の下まで配線が可能となり第１の導電配線層の引き回しの自由度が大幅に増し、多層配線構造が実現できる。

【００７９】第３に、絶縁樹脂シートの採用により従来のガラスエポキシ基板やフレキシブルシート等のインターポーザー基板を用いる場合に比べて、機械的強度を第２の導電膜および封止樹脂層で持たせるので極めて薄型の構造を実現できる。

【００８０】第４に、絶縁樹脂として低熱樹脂あるいは超低熱樹脂を用いることで、絶縁樹脂を薄くできるだけでなくその熱抵抗も大幅に低減でき、半導体素子の発熱を直ちに放熱できる。

【００８１】また、本発明の製造方法では以下の利点を有する。

【００８２】第１に、絶縁樹脂シートとして反りを第２の導電膜で解消でき、搬送性等を向上させることができる。

【００８３】第２に、絶縁樹脂に形成する貫通孔を炭酸ガスレーザーで形成するので、その後直ちに多層接続手段のメッキを行え、工程が極めてシンプルとなる。また多層接続手段として銅メッキを用いれば、銅の第１の導電膜および第２の導電膜と同一材料となり、その後の工程がシンプルとなる。

【００８４】第３に、多層接続手段をメッキ膜で実現できるので、第１の導電配線層を形成する前に多層接続手段をマスクなしで形成でき、第１の導電配線層の形成時に同時にパターニングできるので、多層接続手段の形成が極めて容易である。

【００８５】第４に、封止樹脂層形成時まで絶縁樹脂シートの機械的支持を第２の導電膜で行い、第２の導電配線層を形成後は絶縁樹脂シートの機械的支持を封止樹脂層で行うので、絶縁樹脂の機械的な強度は問われずに極めて薄型の実装方法を実現できる。

【００８６】第５に、絶縁樹脂自体が堅いものでも、またフィラーが混入されて堅くなったものあっても、両面を第１および第２の導電膜でカバーされているので、製造工程で絶縁樹脂シート自体のフラット性が高まり、クラックの発生を防止できる。

【００８７】第６に、絶縁樹脂シートは裏面に第２の導電膜が厚く形成されるため、チップのダイボンディング、ワイヤーボンダー、半導体素子の封止のための支持基板として利用できる。しかも、絶縁樹脂材料自身が柔らかい場合でもワイヤーボンディング時のエネルギーの伝搬を向上できワイヤーボンディング性も向上できる。

【図面の簡単な説明】

【図１】　本発明の回路装置を説明する断面図である。

【図２】　本発明の回路装置を説明する平面図である。

【図３】　本発明の回路装置の製造方法を説明する断面図である。

【図４】　本発明の回路装置の製造方法を説明する断面図である。

【図５】　本発明の回路装置の製造方法を説明する断面図である。

【図６】　本発明の回路装置の製造方法を説明する断面図である。

【図７】　本発明の回路装置の製造方法を説明する断面図である。

【図８】　本発明の回路装置の製造方法を説明する断面図である。

【図９】　本発明の回路装置の製造方法を説明する断面図である。

【図１０】　本発明の回路装置の製造方法を説明する断面図である。

【図１１】　本発明の他の回路装置を説明する断面図である。

【図１２】　従来の半導体装置の製造方法を説明する図である。

【図１３】　従来の半導体装置の製造方法を説明する図である。

【図１４】　従来の半導体装置の製造方法を説明する図である。

【図１５】　従来のフレキシブルシートを説明する図である。

【符号の説明】

1	絶縁樹脂シート
2	絶縁樹脂
3	第１の導電膜
4	第２の導電膜
5	第１の導電配線層
6	第２の導電配線層
7	半導体素子
8	オーバーコート樹脂
9	電極パッド
１０	ボンディングパッド
１１	ボンディングワイヤー

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１２	多層接続手段	＊２１	貫通孔
１３	封止樹脂層	２２	メッキ膜
１４	外部電極	２５	絶縁接着樹脂
１５	オーバーコート樹脂	＊	

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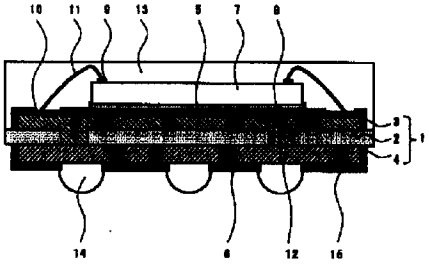
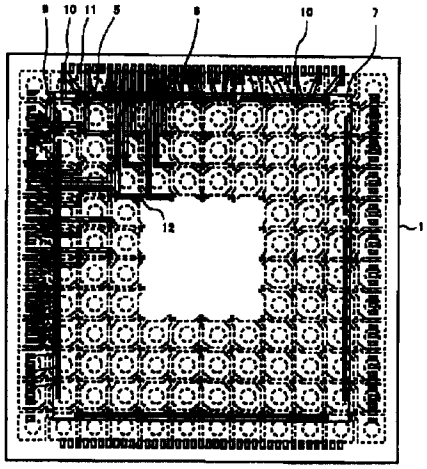
【図１】

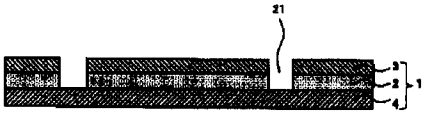


【図２】



【図３】

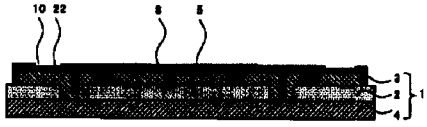
【図４】



【図５】

【図６】

【図７】



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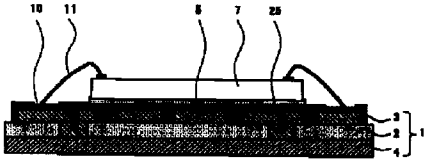

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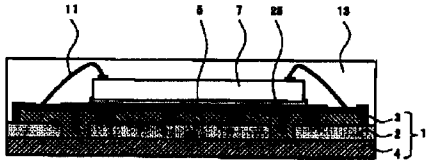
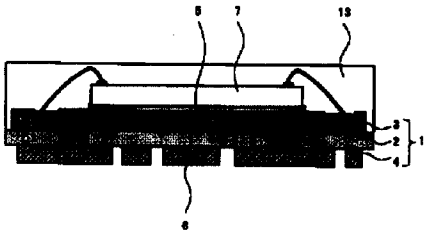
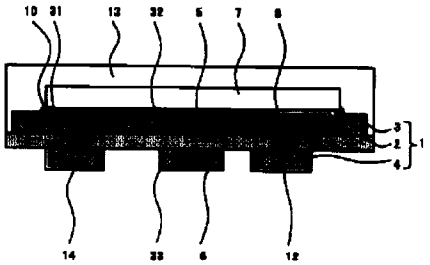


【図１０】



【図１１】



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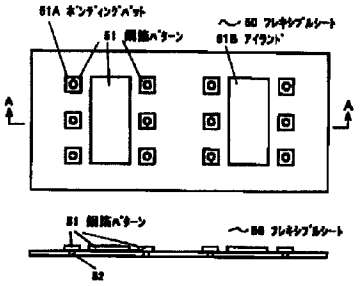
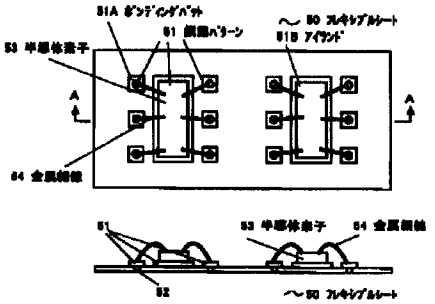
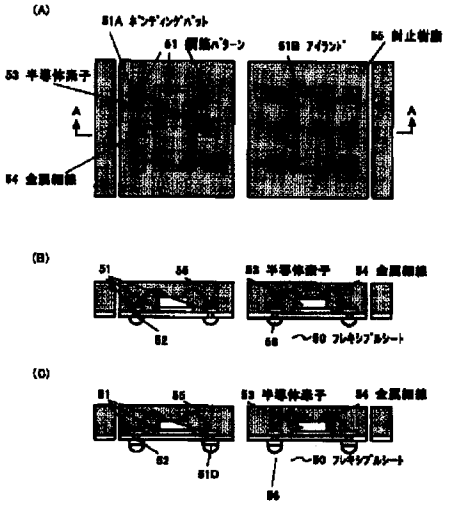


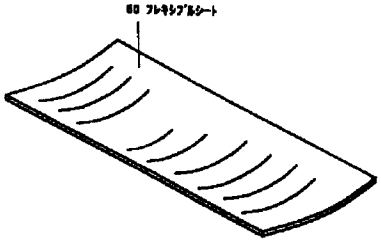
【図１３】



【図１４】



【図１５】



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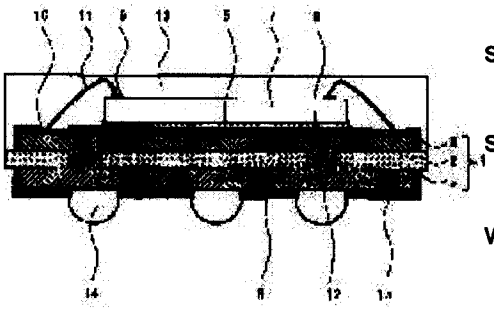
(54) CIRCUIT DEVICE AND MANUFACTURING METHOD THEREFOR

(57)Abstract:



PROBLEM TO BE SOLVED: To overcome such a problem that multiplayer wiring structure cannot be formed and that the warpage of an insulating resin sheet in a manufacturing process is remarkable in a semiconductor device where a flexible sheet having a conductive pattern is adopted as a support substrate, a semiconductor element is mounted on the substrate, and a whole part is molded.

SOLUTION: The insulating resin sheet where a first conductive film 3 and a second conductive film 4 are laminated by insulating resin 2 is used and a first conductive wiring layer 5 is formed by the first conductive film 3. A second conductive wiring layer 6 is formed by the second conductive film 4. Both layers are connected by a multiplayer connection means 12. The semiconductor element 7 is fixed onto overcoat resin 8 covering the first conductive wiring layer 5. Thus, multiplayer wiring structure is realized by the first conductive wiring layer 5 and the second conductive wiring layer 6. Since the second conductive

film 4 formed thick exists, the warpage caused by the difference of the coefficients of thermal expansion can be prevented.

LEGAL STATUS

[Date of request for examination]

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[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against

examiner's decision of rejection]

[Date of extinction of right]

JP 2003-007921 A

English Translation

CLAIMS

[Claim(s)]

[Claim 1] The insulating resin on which the 1st electric conduction film, the 2nd electric conduction film, and said 1st electric conduction film and said 2nd electric conduction film are pasted up in the shape of a sheet, The 1st electric conduction wiring layer which etched said 1st electric conduction film and was formed, The 2nd electric conduction wiring layer which etched said 2nd electric conduction film and was formed, The semiconductor device which is insulated electrically and fixes on said 1st electric conduction wiring layer, The multilayer connecting means which penetrates said insulating resin and is connected in the part of a request of said 1st electric conduction wiring layer and said 2nd electric conduction wiring layer, The circuit apparatus characterized by providing the external electrode prepared in the request part of the closure resin layer which covers said the 1st electric conduction wiring layer and said semiconductor device, and said 2nd electric conduction wiring layer.

[Claim 2] Said 2nd electric conduction film is a circuit apparatus according to claim 1 characterized by forming more thickly than the 1st electric conduction film, and giving support reinforcement.

[Claim 3] Said insulating resin is a circuit apparatus according to claim 1 characterized by using polyimide resin or an epoxy resin as a principal component.

[Claim 4] Said insulating resin is a circuit apparatus according to claim 1 characterized by being thinner than said 2nd electric conduction film.

[Claim 5] Said semiconductor device is a circuit apparatus according to claim 1 characterized by fixing on the overcoat resin which covers said 1st electric conduction wiring layer top.

[Claim 6] Said multilayer connecting means is a circuit apparatus according to claim 1 characterized by being the plating film of an electric conduction metal.

[Claim 7] The circuit apparatus according to claim 1 characterized by preparing the external electrode which consists of solder in the request part which covered said most 2nd electric conduction wiring layer with overcoat resin, and was exposed from this overcoat resin.

[Claim 8] The process for which the insulating resin sheet on which the 1st electric conduction film and the 2nd electric conduction film were pasted up by insulating resin is prepared, The process which forms a through tube in the request part of said insulating resin sheet at said the 1st electric conduction film and said insulating resin, and exposes alternatively the rear face of said 2nd electric conduction film, The process which forms a multilayer connecting means in said through tube, and connects electrically said 1st electric conduction film and said 2nd electric conduction film, The process which etches into the pattern of a request of said 1st electric conduction film, and forms the 1st electric conduction wiring layer, The process which insulates electrically and fixes a semiconductor device on said 1st electric conduction wiring layer, The process which covers said the 1st electric conduction wiring layer and said semiconductor device with a closure resin layer, The manufacture approach of the circuit apparatus characterized by providing the process which etches into the pattern of a request of said 2nd electric conduction film, and forms the 2nd electric conduction wiring layer, and the process which forms an external electrode in the request part of said 2nd electric conduction wiring layer.

[Claim 9] Said 1st electric conduction film and said 2nd electric conduction film are the manufacture approach of the circuit apparatus according to claim 8 characterized by being formed by copper foil.
[Claim 10] Said 1st electric conduction film is the manufacture approach of the circuit apparatus according to claim 8 characterized by being formed more thinly than said 2nd electric conduction film, and carrying out the detailed patternizing of said 1st electric conduction wiring layer.
[Claim 11] Said 2nd electric conduction film is the manufacture approach of the circuit apparatus according to claim 8 characterized by supporting mechanically by said 2nd electric conduction film to the process which it is formed more thickly than said 1st electric conduction film, and is covered with said closure resin layer.
[Claim 12] The manufacture approach of the circuit apparatus according to claim 8 characterized by supporting mechanically in said closure resin layer after the process covered with said closure resin layer.
[Claim 13] Said through tube is the manufacture approach of the circuit apparatus according to claim 8 characterized by carrying out laser etching of said insulating resin by using said 1st electric conduction film as a mask after etching said 1st electric conduction film.
[Claim 14] Said laser etching is the manufacture approach of the circuit apparatus according to claim 13 characterized by using carbon dioxide laser.
[Claim 15] Said multilayer connecting means is the manufacture approach of the circuit apparatus according to claim 8 characterized by being formed in the front face of said through tube and said 1st electric conduction film by non-electric-field plating and electric-field plating of an electric conduction metal.
[Claim 16] The manufacture approach of the circuit apparatus according to claim 8 characterized by leaving a desired part and covering with overcoat resin after forming said 1st electric conduction wiring layer.
[Claim 17] The manufacture approach of the circuit apparatus according to claim 16 characterized by forming the deposit of gold or silver in the part of a request of said 1st electric conduction wiring layer.
[Claim 18] The manufacture approach of the circuit apparatus according to claim 16 characterized by fixing said semiconductor device on said overcoat resin.
[Claim 19] The manufacture approach of the circuit apparatus according to claim 17 characterized by connecting the deposit of the electrode of said semiconductor device, said gold, or silver by the bonding wire.
[Claim 20] Said closure resin layer is the manufacture approach of the circuit apparatus according to claim 8 characterized by being formed by the transfer mold.
[Claim 21] The manufacture approach of the circuit apparatus according to claim 8 characterized by covering said most 2nd electric conduction wiring layer with overcoat resin.
[Claim 22] Said external electrode is the manufacture approach of the circuit apparatus according to claim 8 characterized by adhering, carrying out heating fusion of the solder, and being formed by screen-stencil of solder.
[Claim 23] Said external electrode is the manufacture approach of the circuit apparatus according to claim 8 characterized by being formed by the reflow of solder.
[Claim 24] Said external electrode is the manufacture approach of the circuit apparatus according to claim 8 which etches into the pattern of a request of said 2nd electric conduction film, and is characterized for the front face by gold or carrying out palladium plating and being formed.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention relates to the circuit apparatus which can also realize a multilayer interconnection with the thin shape using the electric conduction film of two sheets, and its manufacture approach about a circuit apparatus and its manufacture approach.

[0002]

[Description of the Prior Art] In recent years, the adoption to a pocket device, or small and a high-density-assembly device tends to progress, and the IC package tends to change a conventional IC package and its conventional mounting concept a lot. For example, it is stated to JP,2000-133678,A. This is a technique about the semiconductor device which adopted the polyimide resin sheet which is a flexible sheet as an example of an insulating resin sheet.

[0003] The flexible sheet 50 is used for drawing 12 - drawing 14 as an INTAPOZA substrate. In addition, the drawing which shows the drawing shown on each drawing to a top view and the bottom is the sectional view of an A-A line.

[0004] On the flexible sheet 50 first shown in drawing 12 , the copper foil pattern 51 is set [it sticks it and] and prepared through adhesives. Although that pattern changes [the semiconductor device in which this copper foil pattern 51 is mounted] with a transistor and ICs, generally bonding pad 51A and island 51B are formed. Moreover, a sign 52 is opening for taking out an electrode from the rear face of the flexible sheet 50, and said copper foil pattern 51 has exposed it.

[0005] Then, this flexible sheet 50 is conveyed by the die bonder, and a semiconductor device 53 is mounted like drawing 13 . Then, this flexible sheet 50 is conveyed by the wire bonder, and the pad of a semiconductor device 53 is electrically connected with bonding pad 51A with the metal thin line 54.

[0006] Finally, the closure of the closure resin 55 is prepared and carried out to the front face of the flexible sheet 50 like drawing 14 (A). Here, a transfer mold is carried out so that bonding pad 51A, island 51B, a semiconductor device 53, and the metal thin line 54 may be covered.

[0007] Then, as shown in drawing 14 (B), the connecting means 56 of solder, a solder ball, etc. is established, and the spherical solder 56 welded to bonding pad 51A through opening 52 by passing through a solder reflow furnace is formed. And since a semiconductor device 53 is formed in the flexible sheet 50 in the shape of a matrix, dicing is carried out like drawing 14 and it dissociates separately.

[0008] Moreover, as for the sectional view shown in drawing 14 (C), 51A and 51D are formed in both sides of the flexible sheet 50 as an electrode. Generally, patterning of both sides is carried out and this flexible sheet 50 is supplied by the manufacturer.

[0009]

[Problem(s) to be Solved by the Invention] Since the semiconductor device using the flexible sheet 50 mentioned above did not use a well-known metal frame, it had the advantage which can realize very small thin package structure, but since it wired only by the copper foil pattern 51 of one layer substantially prepared in the front face of the flexible sheet 50, there was a trouble that multilayer-interconnection structure was unrealizable.

[0010] Moreover, in order to maintain support reinforcement for realizing multilayer-interconnection structure, the flexible sheet 50 needed to be made thick enough with about 200 micrometers, and it also had the trouble which moves against thin shape-ization.

[0011] Furthermore, in the manufacture approach, in the manufacturing installation mentioned above, for example, die BONTA, a wire bonder, transfer molding equipment, a reflow furnace, etc., the flexible sheet 50 is conveyed and the part called a stage or table is equipped.
[0012] However, when thickness of the insulating resin used as the base of the flexible sheet 50 was made thin with about 50 micrometers, 9-35 micrometers and when thin, the thickness of the copper foil pattern 51 formed in a front face also curved, as shown in drawing 15 , and the fault with the bad wearing nature to the stage and table which conveyance nature was very bad and mentioned above had it. This can consider the curvature which depends since insulating resin itself is very thin, and the curvature by the difference with the coefficient of thermal expansion of the copper foil pattern 51 and insulating resin. As shown in drawing 15 , when the hard insulating material without especially the core material of glass-fabrics fiber had curved, there was a trouble of being simply divided in the pressurization from a top.
[0013] Moreover, since the part of opening 52 was pressurized from a top in the case of mold, the force which curves the circumference of bonding pad 51A upwards works, and it might worsen the adhesive property of bonding pad 51A.
[0014] Moreover, it will become hard, if a filler is mixed in order for there to be no flexible nature in the resin ingredient itself which constitutes the flexible sheet 50 or to raise thermal conductivity. If bonding is carried out by the wire bonder in this condition, a crack may go into a part for a bonding area. Moreover, a crack may enter in the part which metal mold contacts also in the case of a transfer mold. If this has curvature as shown in drawing 15 , it will appear more notably.
[0015] Although an electrode was not formed in the rear face, as the flexible sheet 50 explained until now is shown in drawing 14 (C), electrode 51D may be formed also in the rear face of the flexible sheet 50. Since electrode 51D contacted said manufacturing installation or contacted the conveyance side of the conveyance means between this manufacturing installation at this time, the problem which damage generates was in the rear face of electrode 51D. Since it changed as an electrode, with this damage entered, when heat was added behind, there was also a trouble that a crack went into the electrode 51D itself.
[0016] Moreover, when electrode 51D is prepared in the rear face of the flexible sheet 50, in case it is a transfer mold, the trouble which cannot carry out field contact occurs on a stage. In this case, if the flexible sheet 50 changed with a hard ingredient as mentioned above, since electrode 51D would serve as the supporting point and the perimeter of electrode 51D would be pressurized caudad, there was a trouble of making the flexible sheet 50 generating a crack.
[0017]
[Means for Solving the Problem] This invention is made in view of the above-mentioned technical problem. To the 1st on structure The insulating resin on which the 1st electric conduction film, the 2nd electric conduction film, and said 1st electric conduction film and said 2nd electric conduction film are pasted up in the shape of a sheet, The 1st electric conduction wiring layer which etched said 1st electric conduction film and was formed, The 2nd electric conduction wiring layer which etched said 2nd electric conduction film and was formed, The semiconductor device which is insulated electrically and fixes on said 1st electric conduction wiring layer, The multilayer connecting means which penetrates said insulating resin and is connected in the part of a request of said 1st electric conduction wiring layer and said 2nd electric conduction wiring layer, It solves with the circuit apparatus possessing the external electrode prepared in the request part of the closure resin layer which covers said the 1st electric

conduction wiring layer and said semiconductor device, and said 2nd electric conduction wiring layer.
[0018] While insulating electrically the 1st electric conduction film and the 2nd electric conduction film by very thin insulating resin, the sheet unified physically was realized, the 1st electric conduction wiring layer was formed by the 1st electric conduction film, the 2nd electric conduction wiring layer was formed by the 2nd electric conduction film, the 1st electric conduction wiring layer and the 2nd electric conduction wiring layer were connected by the multilayer connecting means, and multilayer-interconnection structure is realized.
[0019] Moreover, since it insulates with the 1st electric conduction wiring layer electrically and a semiconductor device fixes by overcoat resin, the 1st electric conduction wiring layer is freely taken about in the semiconductor device lower part, and is made by it in it.
[0020] The process which prepares the circuit board which pasted up the 1st electric conduction film and the 2nd electric conduction film by insulating resin for the 2nd on the manufacture approach, The process which forms a through tube in the request part of said circuit board at said the 1st electric conduction film and said insulating resin, and exposes said 2nd electric conduction film alternatively, The process which forms a multilayer connecting means in said through tube, and connects electrically said 1st electric conduction film and said 2nd electric conduction film, The process which etches into the pattern of a request of said 1st electric conduction film, and forms the 1st electric conduction wiring layer, The process which insulates electrically and fixes a semiconductor device on said 1st electric conduction wiring layer, The process which covers said the 1st electric conduction wiring layer and said semiconductor device with a closure resin layer, The above-mentioned technical problem is solved by providing the process which etches into the pattern of a request of said 2nd electric conduction film, and forms the 2nd electric conduction wiring layer, and the process which forms an external electrode in the request part of said 2nd electric conduction wiring layer.
[0021] Since it is thickly formed by the 1st electric conduction film and the 2nd electric conduction film, even if insulating resin is thin, the flat nature of the sheet-like circuit board is maintainable.
[0022] Moreover, since the process which covers the 1st electric conduction wiring layer and semiconductor device with a closure resin layer gives a mechanical strength by the 2nd electric conduction film and gives a mechanical strength in a closure resin layer after that, it can form the 2nd electric conduction wiring layer easily by the 2nd electric conduction film. As a result, insulating resin is unnecessary and can make a mechanical strength thin to the thickness which can hold an electric insulation.
[0023] Furthermore, since the 2nd whole electric conduction film can be contacted in the Shimokane mold and field of transfer molding equipment, local pressurization is lost and the crack initiation of insulating resin can be inhibited.
[0024] Furthermore, since the 1st electric conduction film forms the 1st electric conduction wiring layer after forming a multilayer connecting means in a through tube, a multilayer connecting means can be formed without a mask again.
[0025]
[Embodiment of the Invention] The circuit apparatus explaining a circuit apparatus which depends on gestalt this invention of the 1st operation The insulating resin 2 on which the 1st electric conduction film 3, the 2nd electric conduction film 4, and said 1st electric conduction film 3 and said 2nd electric conduction film 4 are pasted up in the shape of a sheet as shown in drawing 1 , The 1st electric conduction wiring layer 5 which etched said 1st electric conduction

film 3, and was formed, The 2nd electric conduction wiring layer 6 which etched said 2nd electric conduction film 4, and was formed, The semiconductor device 7 which is insulated electrically and fixes on said 1st electric conduction wiring layer 5, The multilayer connecting means 12 which penetrates said insulating resin 2 and is connected in the part of a request of said 1st electric conduction wiring layer 5 and said 2nd electric conduction wiring layer 6, It consists of external electrodes 14 prepared in the request part of the closure resin layer 13 which covers said the 1st electric conduction wiring layer 5 and said semiconductor device 7, and said 2nd electric conduction wiring layer 6.

[0026] An insulating resin sheet is explained first. The whole is the insulating resin sheet 1 and, as for drawing 3 , insulating resin 2 is formed in the middle. The 1st electric conduction film 3 is formed in the front face of this insulating resin 2, and the 2nd electric conduction film 4 is formed in a rear face.

[0027] That is, the 1st electric conduction film 3 is formed in the front face of the insulating resin sheet 1 throughout parenchyma, and the 2nd electric conduction film 4 is formed also in a rear face throughout parenchyma. Moreover, the ingredient of insulating resin 2 changes by the insulating material which consists of macromolecules, such as polyimide resin or an epoxy resin. Moreover, the 1st electric conduction film 3 and the 2nd electric conduction film 4 are the ingredients of the thing which makes Cu the charge of a principal member, or a well-known leadframe preferably, it may be covered with plating, vacuum deposition, or a spatter by insulating resin 2, or the metallic foil formed by the rolling-out method or plating may be stuck.

[0028] Moreover, the insulating resin sheet 1 may be formed by the casting method. The manufacture approach is described briefly [below]. Pastiness polyimide resin is first applied on the 1st flat film-like electric conduction film, and pastiness polyimide resin is applied also on the 2nd flat film-like electric conduction film. And if it sticks after carrying out semi-hardening of both polyimide, the insulating resin sheet 1 will be done. Therefore, the glass-fabrics fiber for reinforcement is made unnecessary at the insulating resin sheet 1.

[0029] The point by which it is characterized [of this invention] is in the place which forms the 2nd electric conduction film 4 more thickly than the 1st electric conduction film 3.

[0030] The 1st electric conduction film 3 is considered so that it is formed in about 5-35 micrometers, and thickness may make it as thin as possible and can form a fine pattern. The 2nd electric conduction film 4 has good thickness at about 70-200 micrometers, and the point of giving support reinforcement is thought as important.

[0031] Therefore, by forming the 2nd electric conduction film 4 thickly, the surface smoothness of the insulating resin sheet 1 can be maintained, the workability of a next process can be raised, and induction of the defect to insulating resin 2, a crack, etc. can be prevented.

[0032] Moreover, since closure resin can be hardened maintaining surface smoothness, the rear face of PAKEJJI can also be made flat and the electrode formed in the rear face of the insulating resin sheet 1 can also be arranged for a flat. Therefore, the electrode on a mounting substrate and the electrode of insulating resin sheet 1 rear face can be contacted, and poor solder can be prevented.

[0033] Insulating resin 2 has polyimide resin, a desirable epoxy resin, etc. In the case of the casting method which applies a paste-like thing and is used as a sheet, the thickness is 10 micrometers - about 100 micrometers. Moreover, when forming as a sheet, a commercial thing is the thickness of min 25 micrometers. Moreover, thermal conductivity may be taken into consideration and a filler may be mixed in inside. As an ingredient, glass, Oxidization Si, an aluminum oxide, Nitriding aluminum, Si carbide, boron nitride, etc. can be considered.

[0034] Thus, insulating resin 2 can be chosen with the low-fever resistance resin, super-low-fever resistance resin, or polyimide resin which mixed the filler mentioned above, and can be properly used with the property of the circuit apparatus to form.
[0035] The 1st electric conduction wiring layer 5 etches the 1st electric conduction film 3, and is formed. The 1st electric conduction wiring layer 5 to which thickness is formed in about 5-35 micrometers, and the 1st electric conduction film 3 extends in the center from a bonding pad 10 and this bonding pad 10 on the outskirts by etching is formed. If the number of pads of the semiconductor device carried increases, fine patternizing will be required indeed.
[0036] The 2nd electric conduction wiring layer 6 etches the 2nd electric conduction film, and is formed. Although the thickness of the 2nd electric conduction film 4 is 70 micrometers - about 200 micrometers and is not suitable for a fine pattern, its formation of the external electrode 14 is main, and it can form a multilayer interconnection if needed.
[0037] A semiconductor device 7 fixes with adhesives on the overcoat resin 8 which covers the 1st electric conduction wiring layer 5 top, and a semiconductor device 7 and the 1st electric conduction wiring layer 5 are insulated electrically. Consequently, the 1st electric conduction wiring layer 5 of a fine pattern can wire the bottom of a semiconductor device 7 freely, and the degree of freedom of wiring increases sharply. Each electrode pad 9 of a semiconductor device 7 is connected to the bonding pad 10 which is a part of 1st electric conduction wiring layer 5 prepared on the outskirts by the bonding wire 11. In addition, gold or silver plating is given to the front face so that a bonding pad 10 can perform bonding.
[0038] The multilayer connecting means 12 penetrated insulating resin 2, and is connected in the part of a request of the 1st electric conduction wiring layer 5 and the 2nd electric conduction wiring layer 6. As a multilayer-interconnection means 12, the copper plating film is specifically suitable. Moreover, plating film, such as gold, silver, and PARAJUUMU, is sufficient.
[0039] The closure resin layer 13 has covered the 1st electric conduction wiring layer 5 and semiconductor device 7. Work of mechanical support of the completed circuit apparatus is also making this closure resin layer 13 serve a double purpose.
[0040] The external electrode 14 is formed in the request part of the 2nd electric conduction wiring layer 6. That is, the greater part of 2nd electric conduction wiring layer 6 is covered with overcoat resin 15, and it forms the external electrode 14 formed with solder on the 2nd exposed electric conduction wiring layer 6.
[0041] The circuit apparatus of materialized this invention is explained with reference to drawing 2 . First, the pattern shown as a continuous line is the 1st electric conduction wiring layer 5, and the pattern shown by the dotted line is the 2nd electric conduction wiring layer 6. A bonding pad 10 is formed on the outskirts, and the 1st electric conduction wiring layer 5 is partly equivalent to the semiconductor device 7 which is arranged in two steps and has many pads so that a semiconductor device 7 may be surrounded. It connects with the electrode pad 9 with which a semiconductor device 7 corresponds by the bonding wire 11, and many 1st electric conduction wiring layer 5 of a fine pattern extends under a semiconductor device 7 from a bonding pad 10, and the bonding pad 10 is connected with the 2nd electric conduction wiring layer 6 by the multilayer connecting means 12 shown by the black dot.
[0042] If it is this structure, also by the semiconductor device which has or more 200 pad, it can extend with multilayer-interconnection structure to the 2nd desired electric conduction wiring layer 6 using the fine pattern of the 1st electric conduction wiring layer 5, and connection with the external circuit established in the 2nd electric conduction wiring layer 6 from the external electrode 14 can be made. The manufacture approach of the circuit apparatus of gestalt this

invention the 2nd operation explaining the manufacture approach of a circuit apparatus is explained with reference to drawing 1 - drawing 10 .
[0043] The process which the manufacture approach of the circuit apparatus of this invention prepares the insulating resin sheet 1 on which the 1st electric conduction film 3 and the 2nd electric conduction film 4 were pasted up by insulating resin 2, The process which forms a through tube 21 in the request part of said insulating resin sheet 1 at said the 1st electric conduction film 3 and said insulating resin 2, and exposes alternatively the rear face of said 2nd electric conduction film 4, The process which forms the multilayer connecting means 12 in said through tube 21, and connects electrically said 1st electric conduction film 3 and said 2nd electric conduction film 4, The process which etches into the pattern of a request of said 1st electric conduction film 3, and forms the 1st electric conduction wiring layer 5, The process which insulates electrically and fixes a semiconductor device 7 on said 1st electric conduction wiring layer 5, The process which covers said the 1st electric conduction wiring layer 5 and said semiconductor device 7 with the closure resin layer 13, It consists of a process which etches into the pattern of a request of said 2nd electric conduction film 4, and forms the 2nd electric conduction wiring layer 6, and a process which forms the external electrode 14 in the request part of said 2nd electric conduction wiring layer 6.
[0044] The 1st process of this invention is to prepare the insulating resin sheet 1 on which the 1st electric conduction film 3 and the 2nd electric conduction film 4 were pasted up by insulating resin 2, as shown in drawing 3 .
[0045] The 1st electric conduction film 3 is formed throughout parenchyma, and, as for the front face of the insulating resin sheet 1, the 2nd electric conduction film 4 is formed also in a rear face throughout parenchyma. Moreover, the ingredient of insulating resin 2 changes by the insulating material which consists of macromolecules, such as polyimide resin or an epoxy resin. Moreover, the 1st electric conduction film 3 and the 2nd electric conduction film 4 are the ingredients of the thing which makes Cu the charge of a principal member, or a well-known leadframe preferably, it may be covered with plating, vacuum deposition, or a spatter by insulating resin 2, or the metallic foil formed by the rolling-out method or plating may be stuck.
[0046] Moreover, the insulating resin sheet 1 may be formed by the casting method. The manufacture approach is described briefly [below]. Pastiness polyimide resin is first applied on the 1st flat film-like electric conduction film 3, and pastiness polyimide resin is applied also on the 2nd flat film-like electric conduction film 4. And if it sticks after carrying out semi-hardening of both polyimide resin, the insulating resin sheet 1 will be done.
[0047] The point by which it is characterized [of this invention] is in the place which forms the 2nd electric conduction film 4 more thickly than the 1st electric conduction film 3.
[0048] The 1st electric conduction film 3 is considered so that it is formed in about 5-35 micrometers, and thickness may make it as thin as possible and can form a fine pattern. The 2nd electric conduction film 4 has good thickness at about 70-200 micrometers, and the point of giving support reinforcement is thought as important.
[0049] Insulating resin 2 has polyimide resin, a desirable epoxy resin, etc. In the case of the casting method which applies a paste-like thing and is used as a sheet, the thickness is 10 micrometers - about 100 micrometers. Moreover, when forming as a sheet, a commercial thing is the thickness of min 25 micrometers. Moreover, thermal conductivity may be taken into consideration and a filler may be mixed in inside. As an ingredient, glass, Oxidization Si, an aluminum oxide, Nitriding aluminum, Si carbide, boron nitride, etc. can be considered.

[0050] Thus, insulating resin 2 can be chosen with the low-fever resistance resin, super-low-fever resistance resin, or polyimide resin which mixed the filler mentioned above, and can be properly used with the property of the circuit apparatus to form.
[0051] As shown in drawing 4 , the 2nd process of this invention forms a through tube 21 in the request part of the insulating resin sheet 1 at the 1st electric conduction film 3 and insulating resin 2, and is to expose the 2nd electric conduction film 4 alternatively.
[0052] Only the part which forms the through tube 21 of the 1st electric conduction film 3 is exposed, and the whole surface is covered with a photoresist. And the 1st electric conduction film 3 is etched through this photoresist. Since the 1st electric conduction film 3 makes Cu the charge of a principal member, an etching reagent performs chemical etching using ferric chloride or cupric chloride. Although the diameter of opening of a through tube 21 changes with the resolution of phot lithography, it is about 50-100 micrometers here. Moreover, in the case of this etching, the 2nd electric conduction film 4 is covered with an adhesive sheet etc., and is protected from an etching reagent. However, the 2nd electric conduction film 4 the very thing is fully thick, and as long as it is the thickness which can maintain surface smoothness also after etching, it may be etched a little. In addition, as 1st electric conduction film 3, aluminum, Fe, Fe-nickel, well-known leadframe material, etc. are sufficient.
[0053] Then, after removing a photoresist, the 1st electric conduction film 3 is used as a mask, the insulating resin 2 just under a through tube 21 is removed with laser, and the rear face of the 2nd electric conduction film 4 is exposed at the bottom of a through tube 21. As laser, carbon dioxide laser is desirable. Moreover, when residue is in the pars basilaris ossis occipitalis of opening after evaporating insulating resin by laser, wet etching is carried out with permanganic acid soda or ammonium persulfate, and this residue is removed.
[0054] In addition, at this process, when the 1st electric conduction film 3 is as thin as about 10 micrometers, after covering with a photoresist except through tube 21, the 1st electric conduction film 3 and insulating resin 2 are put in block by carbon dioxide laser, and a through tube 21 can be formed. in this case, the melanism which roughens the front face of the 1st electric conduction film 3 beforehand -- down stream processing is required.
[0055] As shown in drawing 5 , the 3rd process of this invention forms the multilayer connecting means 12 in a through tube 21, and is to connect electrically the 1st electric conduction film 3 and the 2nd electric conduction film 4.
[0056] The plating film which is the multilayer connecting means 12 which performs electrical installation of the 2nd electric conduction film 4 and the 1st electric conduction film 3 all over electric conduction film of ** 1st containing through tube 21 3 is formed. This plating film is formed by both electroless deposition and electrolytic plating, and forms about 2-micrometer Cu by electroless deposition here all over electric conduction film of ** 1st which contains through tube 21 at least 3. Since the 1st electric conduction film 3 and the 2nd electric conduction film 4 flow electrically by this, these 1st and 2nd electric conduction film 3 and 4 is again used as an electrode, electrolytic plating is performed, and about 20-micrometer Cu is plated. Thereby, a through tube 21 is embedded by Cu and the multilayer connecting means 12 is formed. In addition, if plating liquid called an EBARAYUJI light is adopted by the trade name, it is also possible to embed only a through tube 21 alternatively. Moreover, although Cu was used for the plating film here, Au, Ag, Pd, etc. may be used for it. Moreover, parcel plating may be carried out using a mask.

[0057] The 4th process of this invention is to etch into the pattern of a request of the 1st electric conduction film 3, and form the 1st electric conduction wiring layer 5, as shown in drawing 6 and drawing 7 .
[0058] On the 1st electric conduction film 3, it covers with the photoresist of a desired pattern and the 1st electric conduction wiring layer 5 which extends in the center from a bonding pad 10 and a bonding pad 10 is formed by chemical etching. Since the 1st electric conduction film 3 makes Cu the charge of a principal member, ferric chloride or cupric chloride should just be used for an etching reagent.
[0059] Since thickness is formed in about 5-35 micrometers, the 1st electric conduction film 3 can form the 1st electric conduction wiring layer 5 in a fine pattern 50 micrometers or less.
[0060] Then, the bonding pad 10 of the 1st electric conduction wiring layer 5 is exposed, and other parts are covered with overcoat resin 8. By screen-stencil, overcoat resin 8 adheres and carries out heat curing of the epoxy resin melted with the solvent.
[0061] Moreover, as shown in drawing 7 , on a bonding pad 10, the plating film 22, such as Au and Ag, is formed in consideration of bonding nature. This plating film 22 uses overcoat resin 8 as a mask, and it adheres to it in non-electric-field plating alternatively on a bonding pad 10, or adheres to it in electric-field plating by using the 2nd electric conduction film 4 as an electrode.
[0062] The 5th process of this invention is to insulate electrically and fix a semiconductor device 7 on the 1st electric conduction wiring layer 5, as shown in drawing 8 .
[0063] Die bond of the semiconductor device 7 is carried out by insulating adhesion resin 25 on overcoat resin 8 with a bare chip. Since a semiconductor device 7 and the 1st electric conduction wiring layer 5 under it are electrically insulated by overcoat resin 8, also under a semiconductor device 7, the 1st electric conduction wiring layer 5 can wire freely, and can realize multilayer-interconnection structure.
[0064] Moreover, each electrode pad 9 of a semiconductor device 7 is connected to the bonding pad 10 which is a part of 1st electric conduction wiring layer 5 prepared on the outskirts by the bonding wire 11. A semiconductor device 7 may be mounted by face down. In this case, a solder ball and a bump are prepared in each electrode pad 9 front face of a semiconductor device 7, and a bonding pad 10 and the same electrode are prepared in the front face of the insulating resin sheet 1 at the part corresponding to the location of a solder ball (refer to drawing 11).
[0065] The merit using the insulating resin sheet 1 at the time of wire BONDE ink is described. Generally in the case of wire bonding of Au line, it is heated by 200 degrees C - 300 degrees C. If the 2nd electric conduction film 4 is thin at this time, the insulating resin sheet 1 may carry out crack initiation to the insulating resin sheet 1, if the insulating resin sheet 1 is pressurized through a bonding head in the state of [this] curvature. If a filler is mixed in insulating resin 2, since the ingredient itself will become hard and it will lose flexibility, this appears more notably. Moreover, since resin is soft when it is compared from a metal, by the bonding of Au or aluminum, the energy of pressurization or a supersonic wave will emit it. However, these problems are solvable by the 2nd electric conduction film 4 the very thing being thinly formed thickly in insulating resin 2.
[0066] The 6th process of this invention is to cover the 1st electric conduction wiring layer 5 and semiconductor device 7 with the closure resin layer 13, as shown in drawing 9 .
[0067] The insulating resin sheet 1 is set in mold equipment, and performs resin mold. As the mold approach, a transfer mold, injection molding, spreading, and DIPINGU are also possible. However, if mass-production nature is taken into consideration, a transfer mold and injection molding are suitable.

[0068] At this process, although the insulating resin sheet 1 needs to be contacted by the Shimokane mold of a mold mold cavity in a flat, the 2nd thick electric conduction film 4 carries out this work. And the surface smoothness of a package is maintained with the 2nd electric conduction film 4 until contraction of the closure resin layer 13 is completed completely, even after taking out from a mold mold cavity.
[0069] That is, a role of mechanical support of the insulating resin sheet 1 to this process is played with the 2nd electric conduction film 4.
[0070] The 7th process of this invention is to etch into the pattern of a request of the 2nd electric conduction film 4, and form the 2nd electric conduction wiring layer 6, as shown in drawing 10 .
[0071] The 2nd electric conduction film 4 is covered with the photoresist of a desired pattern, and forms the 2nd electric conduction wiring layer 6 by chemical etching. Although the 2nd electric conduction film 4 does not fit fine patternizing since it is thick, it is the purpose in which most forms the external electrode 14, and is satisfactory. The 2nd electric conduction wiring layer 6 was arranged at fixed spacing, as shown in drawing 2 , it connected electrically through the 1st electric conduction wiring layer 5 and multilayer connecting means 12, and each has realized multilayer-interconnection structure. In addition, as long as it is required, the 2nd electric conduction wiring layer 6 for making the 1st electric conduction wiring layer 5 cross in a margin part may be formed.
[0072] The 8th process of this invention is to form the external electrode 14 in the request part of the 2nd electric conduction wiring layer 6, as shown in drawing 1 .
[0073] The 2nd electric conduction wiring layer 15 screen-stencils the epoxy resin which exposed the part which forms the external electrode 14 and was melted with the solvent, and covers most with overcoat resin 15. Next, the external electrode 14 is formed in this exposed part by the reflow of solder at coincidence.
[0074] Finally, since many circuit apparatus are formed in the insulating resin sheet 1 in the shape of a matrix, the dicing of the closure resin layer 13 and the insulating resin sheet 1 is carried out, and they are divided into each circuit apparatus.
[0075] A semiconductor device 7 shows the structure mounted by the face down to drawing 11 . The component which is common in drawing 1 attaches the same sign. The bump electrode 31 is formed in a semiconductor device 7, and this bump electrode 31 and the Bud electrode 10 are connected. The clearance between overcoat resin 8 and a semiconductor device 7 is filled up with under-filling resin 32. With this structure, a bonding wire can be lost and thickness of the closure resin layer 13 can be made still thinner. Moreover, the external electrode 14 can also attain the bump electrode which etched the 2nd electric conduction film 4 and covered the front face with gold or the palladium plating film 33.
[0076]
[Effect of the Invention] If it depends on this invention, on structure, it has the following advantages.
[0077] Since it is formed thinly, the 1st electric conduction wiring layer can carry out the fine patternizing of the 1st electric conduction film, and the inclusion of 100 or more semiconductor devices of the number of electrode pads becomes possible the 1st.
[0078] Since a semiconductor device and the 1st electric conduction wiring layer can be electrically insulated by overcoat resin to the 2nd, wiring becomes possible under a semiconductor device, the degree of freedom of leading about of the 1st electric conduction wiring layer increases sharply to it, and multilayer-interconnection structure can be realized to it.

[0079] Since a mechanical strength is given to the 3rd in the 2nd electric conduction film and closure resin layer compared with the case where INTAPOZA substrates, such as the conventional glass epoxy group plate and a flexible sheet, are used by adoption of an insulating resin sheet, very thin structure is realizable.
[0080] By using low-fever resin or super-low-fever resin for the 4th as insulating resin, it does not come out of insulating resin as much as possible thinly, and the thermal resistance can also be reduced sharply and can radiate heat immediately in generation of heat of a semiconductor device.
[0081] Moreover, by the manufacture approach of this invention, it has the following advantages.
[0082] To the 1st, curvature can be canceled by the 2nd electric conduction film as an insulating resin sheet, and conveyance nature etc. can be raised to it.
[0083] Since the through tube formed in insulating resin is formed in the 2nd by carbon dioxide laser, a multilayer connecting means can be plated immediately after that, and a process becomes very simple. Moreover, if coppering is used as a multilayer connecting means, it will become the same ingredient as the 1st copper electric conduction film and the 2nd electric conduction film, and a subsequent process will become simple.
[0084] Since a multilayer connecting means can be formed in it without a mask and patterning can be carried out to it at coincidence at the time of formation of the 1st electric conduction wiring layer before forming the 1st electric conduction wiring layer in it, since a multilayer connecting means is realizable for the 3rd with the plating film, formation of a multilayer connecting means is very easy.
[0085] Since the 2nd electric conduction film performs mechanical support of an insulating resin sheet to the 4th till the closure resin stratification, and mechanical support of an insulating resin sheet is performed to it in a closure resin layer after forming the 2nd electric conduction wiring layer, the mechanical reinforcement of insulating resin can realize the very thin mounting approach, without being asked.
[0086] the filler was mixed in the 5th and the thing which has hard insulating resin itself also became hard -- since both sides are covered by the 1st and 2nd electric conduction film even if it is, the flat nature of the insulating resin sheet itself increases by the production process, and generating of a crack can be prevented.
[0087] Since the 2nd electric conduction film is thickly formed in a rear face, an insulating resin sheet can be used for the 6th as a support substrate for the closure of the die bonding of a chip, a wire bonder, and a semiconductor device. And even when the insulating resin ingredient itself is soft, propagation of the energy at the time of wire bonding can be improved, and wire-bonding nature can also improve.

TECHNICAL FIELD

[Field of the Invention] Especially this invention relates to the circuit apparatus which can also realize a multilayer interconnection with the thin shape using the electric conduction film of two sheets, and its manufacture approach about a circuit apparatus and its manufacture approach.

PRIOR ART

[Description of the Prior Art] In recent years, the adoption to a pocket device, or small and a high-density-assembly device tends to progress, and the IC package tends to change a

conventional IC package and its conventional mounting concept a lot. For example, it is stated to JP,2000-133678,A. This is a technique about the semiconductor device which adopted the polyimide resin sheet which is a flexible sheet as an example of an insulating resin sheet.
[0003] The flexible sheet 50 is used for drawing 12 - drawing 14 as an INTAPOZA substrate. In addition, the drawing which shows the drawing shown on each drawing to a top view and the bottom is the sectional view of an A-A line.
[0004] On the flexible sheet 50 first shown in drawing 12 , the copper foil pattern 51 is set [it sticks it and] and prepared through adhesives. Although that pattern changes [the semiconductor device in which this copper foil pattern 51 is mounted] with a transistor and ICs, generally bonding pad 51A and island 51B are formed. Moreover, a sign 52 is opening for taking out an electrode from the rear face of the flexible sheet 50, and said copper foil pattern 51 has exposed it.
[0005] Then, this flexible sheet 50 is conveyed by the die bonder, and a semiconductor device 53 is mounted like drawing 13 . Then, this flexible sheet 50 is conveyed by the wire bonder, and the pad of a semiconductor device 53 is electrically connected with bonding pad 51A with the metal thin line 54.
[0006] Finally, the closure of the closure resin 55 is prepared and carried out to the front face of the flexible sheet 50 like drawing 14 (A). Here, a transfer mold is carried out so that bonding pad 51A, island 51B, a semiconductor device 53, and the metal thin line 54 may be covered.
[0007] Then, as shown in drawing 14 (B), the connecting means 56 of solder, a solder ball, etc. is established, and the spherical solder 56 welded to bonding pad 51A through opening 52 by passing through a solder reflow furnace is formed. And since a semiconductor device 53 is formed in the flexible sheet 50 in the shape of a matrix, dicing is carried out like drawing 14 and it dissociates separately.
[0008] Moreover, as for the sectional view shown in drawing 14 (C), 51A and 51D are formed in both sides of the flexible sheet 50 as an electrode. Generally, patterning of both sides is carried out and this flexible sheet 50 is supplied by the manufacturer.

EFFECT OF THE INVENTION

[Effect of the Invention] If it depends on this invention, on structure, it has the following advantages.
[0077] Since it is formed thinly, the 1st electric conduction wiring layer can carry out the fine patternizing of the 1st electric conduction film, and the inclusion of 100 or more semiconductor devices of the number of electrode pads becomes possible the 1st.
[0078] Since a semiconductor device and the 1st electric conduction wiring layer can be electrically insulated by overcoat resin to the 2nd, wiring becomes possible under a semiconductor device, the degree of freedom of leading about of the 1st electric conduction wiring layer increases sharply to it, and multilayer-interconnection structure can be realized to it.
[0079] Since a mechanical strength is given to the 3rd in the 2nd electric conduction film and closure resin layer compared with the case where INTAPOZA substrates, such as the conventional glass epoxy group plate and a flexible sheet, are used by adoption of an insulating resin sheet, very thin structure is realizable.
[0080] By using low-fever resin or super-low-fever resin for the 4th as insulating resin, it does not come out of insulating resin as much as possible thinly, and the thermal resistance can also

be reduced sharply and can radiate heat immediately in generation of heat of a semiconductor device.
[0081] Moreover, by the manufacture approach of this invention, it has the following advantages.
[0082] To the 1st, curvature can be canceled by the 2nd electric conduction film as an insulating resin sheet, and conveyance nature etc. can be raised to it.
[0083] Since the through tube formed in insulating resin is formed in the 2nd by carbon dioxide laser, a multilayer connecting means can be plated immediately after that, and a process becomes very simple. Moreover, if coppering is used as a multilayer connecting means, it will become the same ingredient as the 1st copper electric conduction film and the 2nd electric conduction film, and a subsequent process will become simple.
[0084] Since a multilayer connecting means can be formed in it without a mask and patterning can be carried out to it at coincidence at the time of formation of the 1st electric conduction wiring layer before forming the 1st electric conduction wiring layer in it, since a multilayer connecting means is realizable for the 3rd with the plating film, formation of a multilayer connecting means is very easy.
[0085] Since the 2nd electric conduction film performs mechanical support of an insulating resin sheet to the 4th till the closure resin stratification, and mechanical support of an insulating resin sheet is performed to it in a closure resin layer after forming the 2nd electric conduction wiring layer, the mechanical reinforcement of insulating resin can realize the very thin mounting approach, without being asked.
[0086] the filler was mixed in the 5th and the thing which has hard insulating resin itself also became hard -- since both sides are covered by the 1st and 2nd electric conduction film even if it is, the flat nature of the insulating resin sheet itself increases by the production process, and generating of a crack can be prevented.
[0087] Since the 2nd electric conduction film is thickly formed in a rear face, an insulating resin sheet can be used for the 6th as a support substrate for the closure of the die bonding of a chip, a wire bonder, and a semiconductor device. And even when the insulating resin ingredient itself is soft, propagation of the energy at the time of wire bonding can be improved, and wire-bonding nature can also improve.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Since the semiconductor device using the flexible sheet 50 mentioned above did not use a well-known metal frame, it had the advantage which can realize very small thin package structure, but since it wired only by the copper foil pattern 51 of one layer substantially prepared in the front face of the flexible sheet 50, there was a trouble that multilayer-interconnection structure was unrealizable.
[0010] Moreover, in order to maintain support reinforcement for realizing multilayer-interconnection structure, the flexible sheet 50 needed to be made thick enough with about 200 micrometers, and it also had the trouble which moves against thin shape-ization.
[0011] Furthermore, in the manufacture approach, in the manufacturing installation mentioned above, for example, die BONTA, a wire bonder, transfer molding equipment, a reflow furnace, etc., the flexible sheet 50 is conveyed and the part called a stage or table is equipped.
[0012] However, when thickness of the insulating resin used as the base of the flexible sheet 50 was made thin with about 50 micrometers, 9-35 micrometers and when thin, the thickness of the copper foil pattern 51 formed in a front face also curved, as shown in drawing 15 , and the fault

with the bad wearing nature to the stage and table which conveyance nature was very bad and mentioned above had it. This can consider the curvature which depends since insulating resin itself is very thin, and the curvature by the difference with the coefficient of thermal expansion of the copper foil pattern 51 and insulating resin. As shown in drawing 15 , when the hard insulating material without especially the core material of glass-fabrics fiber had curved, there was a trouble of being simply divided in the pressurization from a top.

[0013] Moreover, since the part of opening 52 was pressurized from a top in the case of mold, the force which curves the circumference of bonding pad 51A upwards works, and it might worsen the adhesive property of bonding pad 51A.

[0014] Moreover, it will become hard, if a filler is mixed in order for there to be no flexible nature in the resin ingredient itself which constitutes the flexible sheet 50 or to raise thermal conductivity. If bonding is carried out by the wire bonder in this condition, a crack may go into a part for a bonding area. Moreover, a crack may enter in the part which metal mold contacts also in the case of a transfer mold. If this has curvature as shown in drawing 15 , it will appear more notably.

[0015] Although an electrode was not formed in the rear face, as the flexible sheet 50 explained until now is shown in drawing 14 (C), electrode 51D may be formed also in the rear face of the flexible sheet 50. Since electrode 51D contacted said manufacturing installation or contacted the conveyance side of the conveyance means between this manufacturing installation at this time, the problem which damage generates was in the rear face of electrode 51D. Since it changed as an electrode, with this damage entered, when heat was added behind, there was also a trouble that a crack went into the electrode 51D itself.

[0016] Moreover, when electrode 51D is prepared in the rear face of the flexible sheet 50, in case it is a transfer mold, the trouble which cannot carry out field contact occurs on a stage. In this case, if the flexible sheet 50 changed with a hard ingredient as mentioned above, since electrode 51D would serve as the supporting point and the perimeter of electrode 51D would be pressurized caudad, there was a trouble of making the flexible sheet 50 generating a crack.

MEANS

[Means for Solving the Problem] This invention is made in view of the above-mentioned technical problem. To the 1st on structure The insulating resin on which the 1st electric conduction film, the 2nd electric conduction film, and said 1st electric conduction film and said 2nd electric conduction film are pasted up in the shape of a sheet, The 1st electric conduction wiring layer which etched said 1st electric conduction film and was formed, The 2nd electric conduction wiring layer which etched said 2nd electric conduction film and was formed, The semiconductor device which is insulated electrically and fixes on said 1st electric conduction wiring layer, The multilayer connecting means which penetrates said insulating resin and is connected in the part of a request of said 1st electric conduction wiring layer and said 2nd electric conduction wiring layer, It solves with the circuit apparatus possessing the external electrode prepared in the request part of the closure resin layer which covers said the 1st electric conduction wiring layer and said semiconductor device, and said 2nd electric conduction wiring layer.

[0018] While insulating electrically the 1st electric conduction film and the 2nd electric conduction film by very thin insulating resin, the sheet unified physically was realized, the 1st electric conduction wiring layer was formed by the 1st electric conduction film, the 2nd electric

conduction wiring layer was formed by the 2nd electric conduction film, the 1st electric conduction wiring layer and the 2nd electric conduction wiring layer were connected by the multilayer connecting means, and multilayer-interconnection structure is realized.
[0019] Moreover, since it insulates with the 1st electric conduction wiring layer electrically and a semiconductor device fixes by overcoat resin, the 1st electric conduction wiring layer is freely taken about in the semiconductor device lower part, and is made by it in it.
[0020] The process which prepares the circuit board which pasted up the 1st electric conduction film and the 2nd electric conduction film by insulating resin for the 2nd on the manufacture approach, The process which forms a through tube in the request part of said circuit board at said the 1st electric conduction film and said insulating resin, and exposes said 2nd electric conduction film alternatively, The process which forms a multilayer connecting means in said through tube, and connects electrically said 1st electric conduction film and said 2nd electric conduction film, The process which etches into the pattern of a request of said 1st electric conduction film, and forms the 1st electric conduction wiring layer, The process which insulates electrically and fixes a semiconductor device on said 1st electric conduction wiring layer, The process which covers said the 1st electric conduction wiring layer and said semiconductor device with a closure resin layer, The above-mentioned technical problem is solved by providing the process which etches into the pattern of a request of said 2nd electric conduction film, and forms the 2nd electric conduction wiring layer, and the process which forms an external electrode in the request part of said 2nd electric conduction wiring layer.
[0021] Since it is thickly formed by the 1st electric conduction film and the 2nd electric conduction film, even if insulating resin is thin, the flat nature of the sheet-like circuit board is maintainable.
[0022] Moreover, since the process which covers the 1st electric conduction wiring layer and semiconductor device with a closure resin layer gives a mechanical strength by the 2nd electric conduction film and gives a mechanical strength in a closure resin layer after that, it can form the 2nd electric conduction wiring layer easily by the 2nd electric conduction film. As a result, insulating resin is unnecessary and can make a mechanical strength thin to the thickness which can hold an electric insulation.
[0023] Furthermore, since the 2nd whole electric conduction film can be contacted in the Shimokane mold and field of transfer molding equipment, local pressurization is lost and the crack initiation of insulating resin can be inhibited.
[0024] Furthermore, since the 1st electric conduction film forms the 1st electric conduction wiring layer after forming a multilayer connecting means in a through tube, a multilayer connecting means can be formed without a mask again.
[0025]
[Embodiment of the Invention] The circuit apparatus explaining a circuit apparatus which depends on gestalt this invention of the 1st operation The insulating resin 2 on which the 1st electric conduction film 3, the 2nd electric conduction film 4, and said 1st electric conduction film 3 and said 2nd electric conduction film 4 are pasted up in the shape of a sheet as shown in drawing 1 , The 1st electric conduction wiring layer 5 which etched said 1st electric conduction film 3, and was formed, The 2nd electric conduction wiring layer 6 which etched said 2nd electric conduction film 4, and was formed, The semiconductor device 7 which is insulated electrically and fixes on said 1st electric conduction wiring layer 5, The multilayer connecting means 12 which penetrates said insulating resin 2 and is connected in the part of a request of said 1st electric conduction wiring layer 5 and said 2nd electric conduction wiring layer 6, It consists

of external electrodes 14 prepared in the request part of the closure resin layer 13 which covers said the 1st electric conduction wiring layer 5 and said semiconductor device 7, and said 2nd electric conduction wiring layer 6.
[0026] An insulating resin sheet is explained first. The whole is the insulating resin sheet 1 and, as for drawing 3 , insulating resin 2 is formed in the middle. The 1st electric conduction film 3 is formed in the front face of this insulating resin 2, and the 2nd electric conduction film 4 is formed in a rear face.
[0027] That is, the 1st electric conduction film 3 is formed in the front face of the insulating resin sheet 1 throughout parenchyma, and the 2nd electric conduction film 4 is formed also in a rear face throughout parenchyma. Moreover, the ingredient of insulating resin 2 changes by the insulating material which consists of macromolecules, such as polyimide resin or an epoxy resin. Moreover, the 1st electric conduction film 3 and the 2nd electric conduction film 4 are the ingredients of the thing which makes Cu the charge of a principal member, or a well-known leadframe preferably, it may be covered with plating, vacuum deposition, or a spatter by insulating resin 2, or the metallic foil formed by the rolling-out method or plating may be stuck.
[0028] Moreover, the insulating resin sheet 1 may be formed by the casting method. The manufacture approach is described briefly [below]. Pastiness polyimide resin is first applied on the 1st flat film-like electric conduction film, and pastiness polyimide resin is applied also on the 2nd flat film-like electric conduction film. And if it sticks after carrying out semi-hardening of both polyimide, the insulating resin sheet 1 will be done. Therefore, the glass-fabrics fiber for reinforcement is made unnecessary at the insulating resin sheet 1.
[0029] The point by which it is characterized [of this invention] is in the place which forms the 2nd electric conduction film 4 more thickly than the 1st electric conduction film 3.
[0030] The 1st electric conduction film 3 is considered so that it is formed in about 5-35 micrometers, and thickness may make it as thin as possible and can form a fine pattern. The 2nd electric conduction film 4 has good thickness at about 70-200 micrometers, and the point of giving support reinforcement is thought as important.
[0031] Therefore, by forming the 2nd electric conduction film 4 thickly, the surface smoothness of the insulating resin sheet 1 can be maintained, the workability of a next process can be raised, and induction of the defect to insulating resin 2, a crack, etc. can be prevented.
[0032] Moreover, since closure resin can be hardened maintaining surface smoothness, the rear face of PAKEJJI can also be made flat and the electrode formed in the rear face of the insulating resin sheet 1 can also be arranged for a flat. Therefore, the electrode on a mounting substrate and the electrode of insulating resin sheet 1 rear face can be contacted, and poor solder can be prevented.
[0033] Insulating resin 2 has polyimide resin, a desirable epoxy resin, etc. In the case of the casting method which applies a paste-like thing and is used as a sheet, the thickness is 10 micrometers - about 100 micrometers. Moreover, when forming as a sheet, a commercial thing is the thickness of min 25 micrometers. Moreover, thermal conductivity may be taken into consideration and a filler may be mixed in inside. As an ingredient, glass, Oxidization Si, an aluminum oxide, Nitriding aluminum, Si carbide, boron nitride, etc. can be considered.
[0034] Thus, insulating resin 2 can be chosen with the low-fever resistance resin, super-low-fever resistance resin, or polyimide resin which mixed the filler mentioned above, and can be properly used with the property of the circuit apparatus to form.
[0035] The 1st electric conduction wiring layer 5 etches the 1st electric conduction film 3, and is formed. The 1st electric conduction wiring layer 5 to which thickness is formed in about 5-35

micrometers, and the 1st electric conduction film 3 extends in the center from a bonding pad 10 and this bonding pad 10 on the outskirts by etching is formed. If the number of pads of the semiconductor device carried increases, fine patternizing will be required indeed.
[0036] The 2nd electric conduction wiring layer 6 etches the 2nd electric conduction film, and is formed. Although the thickness of the 2nd electric conduction film 4 is 70 micrometers - about 200 micrometers and is not suitable for a fine pattern, its formation of the external electrode 14 is main, and it can form a multilayer interconnection if needed.
[0037] A semiconductor device 7 fixes with adhesives on the overcoat resin 8 which covers the 1st electric conduction wiring layer 5 top, and a semiconductor device 7 and the 1st electric conduction wiring layer 5 are insulated electrically. Consequently, the 1st electric conduction wiring layer 5 of a fine pattern can wire the bottom of a semiconductor device 7 freely, and the degree of freedom of wiring increases sharply. Each electrode pad 9 of a semiconductor device 7 is connected to the bonding pad 10 which is a part of 1st electric conduction wiring layer 5 prepared on the outskirts by the bonding wire 11. In addition, gold or silver plating is given to the front face so that a bonding pad 10 can perform bonding.
[0038] The multilayer connecting means 12 penetrated insulating resin 2, and is connected in the part of a request of the 1st electric conduction wiring layer 5 and the 2nd electric conduction wiring layer 6. As a multilayer-interconnection means 12, the copper plating film is specifically suitable. Moreover, plating film, such as gold, silver, and PARAJUUMU, is sufficient.
[0039] The closure resin layer 13 has covered the 1st electric conduction wiring layer 5 and semiconductor device 7. Work of mechanical support of the completed circuit apparatus is also making this closure resin layer 13 serve a double purpose.
[0040] The external electrode 14 is formed in the request part of the 2nd electric conduction wiring layer 6. That is, the greater part of 2nd electric conduction wiring layer 6 is covered with overcoat resin 15, and it forms the external electrode 14 formed with solder on the 2nd exposed electric conduction wiring layer 6.
[0041] The circuit apparatus of materialized this invention is explained with reference to drawing 2 . First, the pattern shown as a continuous line is the 1st electric conduction wiring layer 5, and the pattern shown by the dotted line is the 2nd electric conduction wiring layer 6. A bonding pad 10 is formed on the outskirts, and the 1st electric conduction wiring layer 5 is partly equivalent to the semiconductor device 7 which is arranged in two steps and has many pads so that a semiconductor device 7 may be surrounded. It connects with the electrode pad 9 with which a semiconductor device 7 corresponds by the bonding wire 11, and many 1st electric conduction wiring layer 5 of a fine pattern extends under a semiconductor device 7 from a bonding pad 10, and the bonding pad 10 is connected with the 2nd electric conduction wiring layer 6 by the multilayer connecting means 12 shown by the black dot.
[0042] If it is this structure, also by the semiconductor device which has or more 200 pad, it can extend with multilayer-interconnection structure to the 2nd desired electric conduction wiring layer 6 using the fine pattern of the 1st electric conduction wiring layer 5, and connection with the external circuit established in the 2nd electric conduction wiring layer 6 from the external electrode 14 can be made. The manufacture approach of the circuit apparatus of gestalt this invention the 2nd operation explaining the manufacture approach of a circuit apparatus is explained with reference to drawing 1 - drawing 10 .
[0043] The process which the manufacture approach of the circuit apparatus of this invention prepares the insulating resin sheet 1 on which the 1st electric conduction film 3 and the 2nd electric conduction film 4 were pasted up by insulating resin 2, The process which forms a

through tube 21 in the request part of said insulating resin sheet 1 at said the 1st electric conduction film 3 and said insulating resin 2, and exposes alternatively the rear face of said 2nd electric conduction film 4, The process which forms the multilayer connecting means 12 in said through tube 21, and connects electrically said 1st electric conduction film 3 and said 2nd electric conduction film 4, The process which etches into the pattern of a request of said 1st electric conduction film 3, and forms the 1st electric conduction wiring layer 5, The process which insulates electrically and fixes a semiconductor device 7 on said 1st electric conduction wiring layer 5, The process which covers said the 1st electric conduction wiring layer 5 and said semiconductor device 7 with the closure resin layer 13, It consists of a process which etches into the pattern of a request of said 2nd electric conduction film 4, and forms the 2nd electric conduction wiring layer 6, and a process which forms the external electrode 14 in the request part of said 2nd electric conduction wiring layer 6.

[0044] The 1st process of this invention is to prepare the insulating resin sheet 1 on which the 1st electric conduction film 3 and the 2nd electric conduction film 4 were pasted up by insulating resin 2, as shown in drawing 3 .

[0045] The 1st electric conduction film 3 is formed throughout parenchyma, and, as for the front face of the insulating resin sheet 1, the 2nd electric conduction film 4 is formed also in a rear face throughout parenchyma. Moreover, the ingredient of insulating resin 2 changes by the insulating material which consists of macromolecules, such as polyimide resin or an epoxy resin. Moreover, the 1st electric conduction film 3 and the 2nd electric conduction film 4 are the ingredients of the thing which makes Cu the charge of a principal member, or a well-known leadframe preferably, it may be covered with plating, vacuum deposition, or a spatter by insulating resin 2, or the metallic foil formed by the rolling-out method or plating may be stuck.

[0046] Moreover, the insulating resin sheet 1 may be formed by the casting method. The manufacture approach is described briefly [below]. Pastiness polyimide resin is first applied on the 1st flat film-like electric conduction film 3, and pastiness polyimide resin is applied also on the 2nd flat film-like electric conduction film 4. And if it sticks after carrying out semi-hardening of both polyimide resin, the insulating resin sheet 1 will be done.

[0047] The point by which it is characterized [of this invention] is in the place which forms the 2nd electric conduction film 4 more thickly than the 1st electric conduction film 3.

[0048] The 1st electric conduction film 3 is considered so that it is formed in about 5-35 micrometers, and thickness may make it as thin as possible and can form a fine pattern. The 2nd electric conduction film 4 has good thickness at about 70-200 micrometers, and the point of giving support reinforcement is thought as important.

[0049] Insulating resin 2 has polyimide resin, a desirable epoxy resin, etc. In the case of the casting method which applies a paste-like thing and is used as a sheet, the thickness is 10 micrometers - about 100 micrometers. Moreover, when forming as a sheet, a commercial thing is the thickness of min 25 micrometers. Moreover, thermal conductivity may be taken into consideration and a filler may be mixed in inside. As an ingredient, glass, Oxidization Si, an aluminum oxide, Nitriding aluminum, Si carbide, boron nitride, etc. can be considered.

[0050] Thus, insulating resin 2 can be chosen with the low-fever resistance resin, super-low-fever resistance resin, or polyimide resin which mixed the filler mentioned above, and can be properly used with the property of the circuit apparatus to form.

[0051] As shown in drawing 4 , the 2nd process of this invention forms a through tube 21 in the request part of the insulating resin sheet 1 at the 1st electric conduction film 3 and insulating resin 2, and is to expose the 2nd electric conduction film 4 alternatively.

[0052] Only the part which forms the through tube 21 of the 1st electric conduction film 3 is exposed, and the whole surface is covered with a photoresist. And the 1st electric conduction film 3 is etched through this photoresist. Since the 1st electric conduction film 3 makes Cu the charge of a principal member, an etching reagent performs chemical etching using ferric chloride or cupric chloride. Although the diameter of opening of a through tube 21 changes with the resolution of phot lithography, it is about 50-100 micrometers here. Moreover, in the case of this etching, the 2nd electric conduction film 4 is covered with an adhesive sheet etc., and is protected from an etching reagent. However, the 2nd electric conduction film 4 the very thing is fully thick, and as long as it is the thickness which can maintain surface smoothness also after etching, it may be etched a little. In addition, as 1st electric conduction film 3, aluminum, Fe, Fe-nickel, well-known leadframe material, etc. are sufficient.
[0053] Then, after removing a photoresist, the 1st electric conduction film 3 is used as a mask, the insulating resin 2 just under a through tube 21 is removed with laser, and the rear face of the 2nd electric conduction film 4 is exposed at the bottom of a through tube 21. As laser, carbon dioxide laser is desirable. Moreover, when residue is in the pars basilaris ossis occipitalis of opening after evaporating insulating resin by laser, wet etching is carried out with permanganic acid soda or ammonium persulfate, and this residue is removed.
[0054] In addition, at this process, when the 1st electric conduction film 3 is as thin as about 10 micrometers, after covering with a photoresist except through tube 21, the 1st electric conduction film 3 and insulating resin 2 are put in block by carbon dioxide laser, and a through tube 21 can be formed. in this case, the melanism which roughens the front face of the 1st electric conduction film 3 beforehand -- down stream processing is required.
[0055] As shown in drawing 5 , the 3rd process of this invention forms the multilayer connecting means 12 in a through tube 21, and is to connect electrically the 1st electric conduction film 3 and the 2nd electric conduction film 4.
[0056] The plating film which is the multilayer connecting means 12 which performs electrical installation of the 2nd electric conduction film 4 and the 1st electric conduction film 3 all over electric conduction film of ** 1st containing through tube 21 3 is formed. This plating film is formed by both electroless deposition and electrolytic plating, and forms about 2-micrometer Cu by electroless deposition here all over electric conduction film of ** 1st which contains through tube 21 at least 3. Since the 1st electric conduction film 3 and the 2nd electric conduction film 4 flow electrically by this, these 1st and 2nd electric conduction film 3 and 4 is again used as an electrode, electrolytic plating is performed, and about 20-micrometer Cu is plated. Thereby, a through tube 21 is embedded by Cu and the multilayer connecting means 12 is formed. In addition, if plating liquid called an EBARAYUJI light is adopted by the trade name, it is also possible to embed only a through tube 21 alternatively. Moreover, although Cu was used for the plating film here, Au, Ag, Pd, etc. may be used for it. Moreover, parcel plating may be carried out using a mask.
[0057] The 4th process of this invention is to etch into the pattern of a request of the 1st electric conduction film 3, and form the 1st electric conduction wiring layer 5, as shown in drawing 6 and drawing 7 .
[0058] On the 1st electric conduction film 3, it covers with the photoresist of a desired pattern and the 1st electric conduction wiring layer 5 which extends in the center from a bonding pad 10 and a bonding pad 10 is formed by chemical etching. Since the 1st electric conduction film 3 makes Cu the charge of a principal member, ferric chloride or cupric chloride should just be used for an etching reagent.

[0059] Since thickness is formed in about 5-35 micrometers, the 1st electric conduction film 3 can form the 1st electric conduction wiring layer 5 in a fine pattern 50 micrometers or less.
[0060] Then, the bonding pad 10 of the 1st electric conduction wiring layer 5 is exposed, and other parts are covered with overcoat resin 8. By screen-stencil, overcoat resin 8 adheres and carries out heat curing of the epoxy resin melted with the solvent.
[0061] Moreover, as shown in drawing 7 , on a bonding pad 10, the plating film 22, such as Au and Ag, is formed in consideration of bonding nature. This plating film 22 uses overcoat resin 8 as a mask, and it adheres to it in non-electric-field plating alternatively on a bonding pad 10, or adheres to it in electric-field plating by using the 2nd electric conduction film 4 as an electrode.
[0062] The 5th process of this invention is to insulate electrically and fix a semiconductor device 7 on the 1st electric conduction wiring layer 5, as shown in drawing 8 .
[0063] Die bond of the semiconductor device 7 is carried out by insulating adhesion resin 25 on overcoat resin 8 with a bare chip. Since a semiconductor device 7 and the 1st electric conduction wiring layer 5 under it are electrically insulated by overcoat resin 8, also under a semiconductor device 7, the 1st electric conduction wiring layer 5 can wire freely, and can realize multilayer-interconnection structure.
[0064] Moreover, each electrode pad 9 of a semiconductor device 7 is connected to the bonding pad 10 which is a part of 1st electric conduction wiring layer 5 prepared on the outskirts by the bonding wire 11. A semiconductor device 7 may be mounted by face down. In this case, a solder ball and a bump are prepared in each electrode pad 9 front face of a semiconductor device 7, and a bonding pad 10 and the same electrode are prepared in the front face of the insulating resin sheet 1 at the part corresponding to the location of a solder ball (refer to drawing 11).
[0065] The merit using the insulating resin sheet 1 at the time of wire BONDE ink is described. Generally in the case of wire bonding of Au line, it is heated by 200 degrees C - 300 degrees C. If the 2nd electric conduction film 4 is thin at this time, the insulating resin sheet 1 may carry out crack initiation to the insulating resin sheet 1, if the insulating resin sheet 1 is pressurized through a bonding head in the state of [this] curvature. If a filler is mixed in insulating resin 2, since the ingredient itself will become hard and it will lose flexibility, this appears more notably. Moreover, since resin is soft when it is compared from a metal, by the bonding of Au or aluminum, the energy of pressurization or a supersonic wave will emit it. However, these problems are solvable by the 2nd electric conduction film 4 the very thing being thinly formed thickly in insulating resin 2.
[0066] The 6th process of this invention is to cover the 1st electric conduction wiring layer 5 and semiconductor device 7 with the closure resin layer 13, as shown in drawing 9 .
[0067] The insulating resin sheet 1 is set in mold equipment, and performs resin mold. As the mold approach, a transfer mold, injection molding, spreading, and DIPINGU are also possible. However, if mass-production nature is taken into consideration, a transfer mold and injection molding are suitable.
[0068] At this process, although the insulating resin sheet 1 needs to be contacted by the Shimokane mold of a mold mold cavity in a flat, the 2nd thick electric conduction film 4 carries out this work. And the surface smoothness of a package is maintained with the 2nd electric conduction film 4 until contraction of the closure resin layer 13 is completed completely, even after taking out from a mold mold cavity.
[0069] That is, a role of mechanical support of the insulating resin sheet 1 to this process is played with the 2nd electric conduction film 4.

[0070] The 7th process of this invention is to etch into the pattern of a request of the 2nd electric conduction film 4, and form the 2nd electric conduction wiring layer 6, as shown in drawing 10 .
[0071] The 2nd electric conduction film 4 is covered with the photoresist of a desired pattern, and forms the 2nd electric conduction wiring layer 6 by chemical etching. Although the 2nd electric conduction film 4 does not fit fine patternizing since it is thick, it is the purpose in which most forms the external electrode 14, and is satisfactory. The 2nd electric conduction wiring layer 6 was arranged at fixed spacing, as shown in drawing 2 , it connected electrically through the 1st electric conduction wiring layer 5 and multilayer connecting means 12, and each has realized multilayer-interconnection structure. In addition, as long as it is required, the 2nd electric conduction wiring layer 6 for making the 1st electric conduction wiring layer 5 cross in a margin part may be formed.
[0072] The 8th process of this invention is to form the external electrode 14 in the request part of the 2nd electric conduction wiring layer 6, as shown in drawing 1 .
[0073] The 2nd electric conduction wiring layer 15 screen-stencils the epoxy resin which exposed the part which forms the external electrode 14 and was melted with the solvent, and covers most with overcoat resin 15. Next, the external electrode 14 is formed in this exposed part by the reflow of solder at coincidence.
[0074] Finally, since many circuit apparatus are formed in the insulating resin sheet 1 in the shape of a matrix, the dicing of the closure resin layer 13 and the insulating resin sheet 1 is carried out, and they are divided into each circuit apparatus.
[0075] A semiconductor device 7 shows the structure mounted by the face down to drawing 11 . The component which is common in drawing 1 attaches the same sign. The bump electrode 31 is formed in a semiconductor device 7, and this bump electrode 31 and the Bud electrode 10 are connected. The clearance between overcoat resin 8 and a semiconductor device 7 is filled up with under-filling resin 32. With this structure, a bonding wire can be lost and thickness of the closure resin layer 13 can be made still thinner. Moreover, the external electrode 14 can also attain the bump electrode which etched the 2nd electric conduction film 4 and covered the front face with gold or the palladium plating film 33.

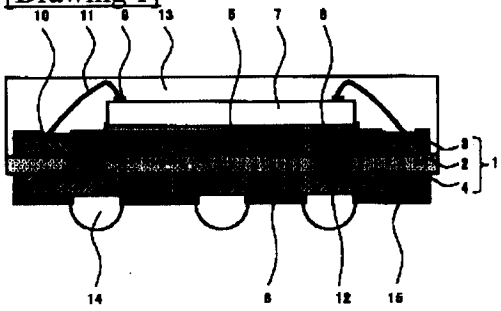
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is a sectional view explaining the circuit apparatus of this invention.
[Drawing 2] It is a top view explaining the circuit apparatus of this invention.
[Drawing 3] It is a sectional view explaining the manufacture approach of the circuit apparatus of this invention.
[Drawing 4] It is a sectional view explaining the manufacture approach of the circuit apparatus of this invention.
[Drawing 5] It is a sectional view explaining the manufacture approach of the circuit apparatus of this invention.
[Drawing 6] It is a sectional view explaining the manufacture approach of the circuit apparatus of this invention.
[Drawing 7] It is a sectional view explaining the manufacture approach of the circuit apparatus of this invention.
[Drawing 8] It is a sectional view explaining the manufacture approach of the circuit apparatus of this invention.

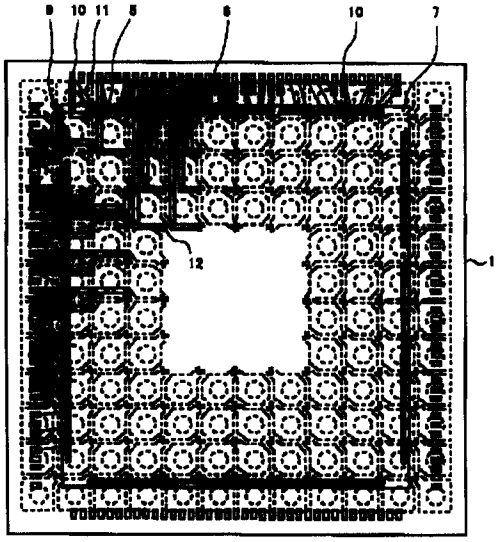
[Drawing 9] It is a sectional view explaining the manufacture approach of the circuit apparatus of this invention.
[Drawing 10] It is a sectional view explaining the manufacture approach of the circuit apparatus of this invention.
[Drawing 11] It is a sectional view explaining other circuit apparatus of this invention.
[Drawing 12] It is drawing explaining the manufacture approach of the conventional semiconductor device.
[Drawing 13] It is drawing explaining the manufacture approach of the conventional semiconductor device.
[Drawing 14] It is drawing explaining the manufacture approach of the conventional semiconductor device.
[Drawing 15] It is drawing explaining the conventional flexible sheet.
[Description of Notations]
1 Insulating Resin Sheet
2 Insulating Resin
3 1st Electric Conduction Film
4 2nd Electric Conduction Film
5 1st Electric Conduction Wiring Layer
6 2nd Electric Conduction Wiring Layer
7 Semiconductor Device
8 Overcoat Resin
9 Electrode Pad
10 Bonding Pad
11 Bonding Wire
12 Multilayer Connecting Means
13 Closure Resin Layer
14 External Electrode
15 Overcoat Resin
21 Through Tube
22 Plating Film
25 Insulating Adhesion Resin

DRAWINGS

[Drawing 1]



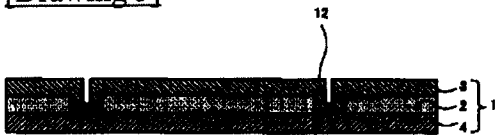
[Drawing 2]



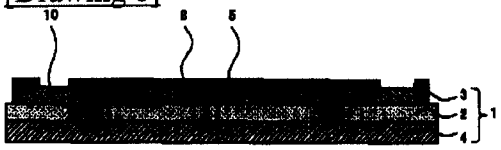
[Drawing 3]

[Drawing 4]

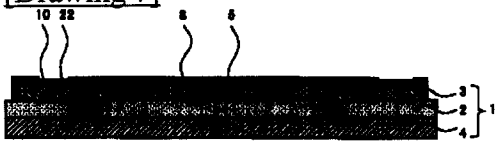
[Drawing 5]



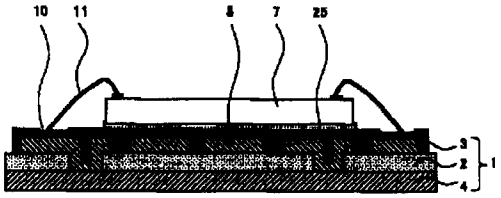
[Drawing 6]



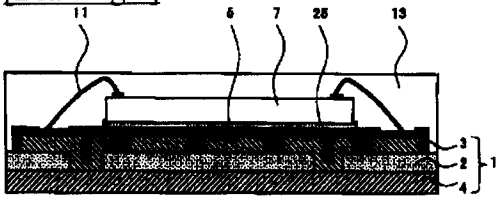
[Drawing 7]



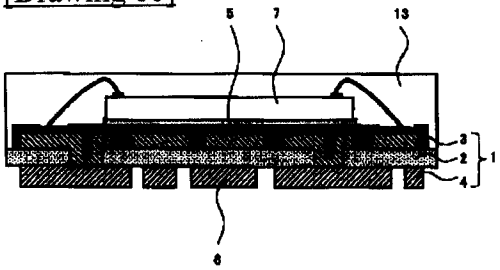
[Drawing 8]



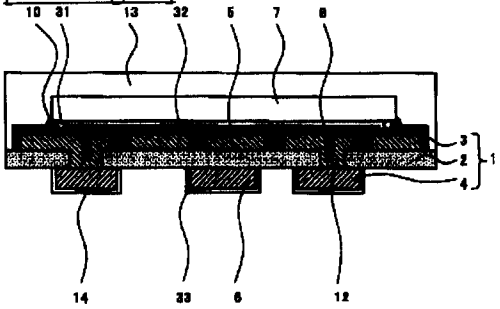
[Drawing 9]



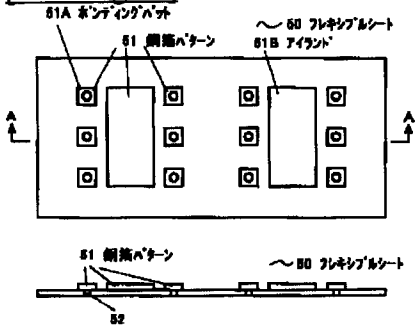
[Drawing 10]



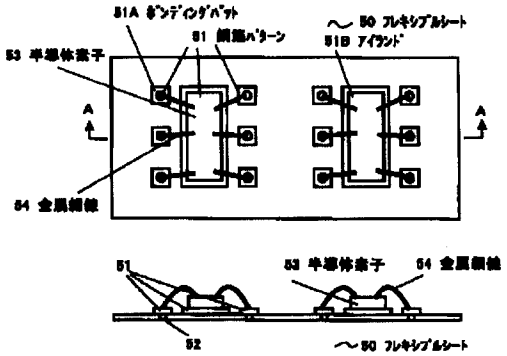
[Drawing 11]



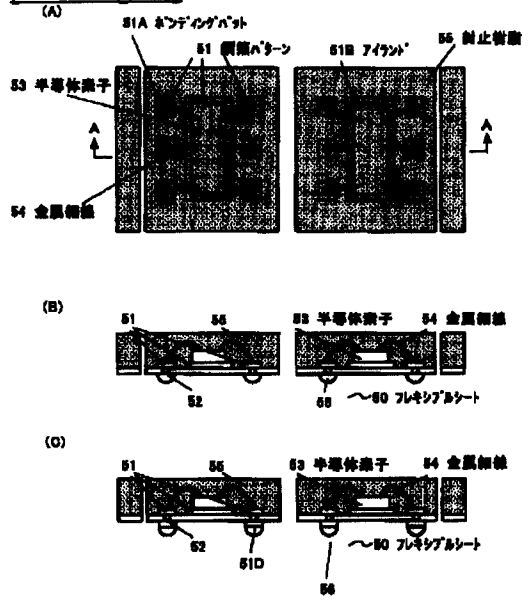
[Drawing 12]



[Drawing 13]



[Drawing 14]



[Drawing 15]